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Delay Analysis for current mode threshold logic gate design

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Abstract:
Threshold logic gates are gaining more importance in recent years due to significant development in switching devices. This renewed the interest in high performance and low power circuits with threshold logic gates. Threshold Logic Gates can be implemented using both the traditional CMOS technologies and the emerging nano electronic technologies. In this dissertation, we have performed performance analysis on Monostable-Bistable Threshold Logic Element based, current mode, and memristor based threshold logic implementations. Existing analytical approaches that model the delay of a Monostable-Bistable Threshold Logic Element threshold logic gate cannot explore the enormous search space in the quest of weight assignments on the inputs and threshold in order to optimize the delay of the threshold logic gate. It is shown that this can be achieved by using a quantity that depends on the constants and Resonant Tunnel Diode weights. This quantity is used to form an integer linear program that optimizes the performance and ensure that each weight can tolerate a predetermined variation by an appropriate weight assignment in a threshold logic gate. The presented experimental results demonstrate the impact of the proposed method. The optimality of our solutions and the reported improvements ensure tolerance to potential manufacturing defects. Current mode is a popular CMOS-based implementation of threshold logic functions where the gate delay depends on the sensor size. A new implementation of current mode threshold functions for improved performance and switching energy is presented. An analytical method is also proposed in order to identify quickly the optimum sensor size. Experimental results on different gates with the optimum sensor size indicate that the proposed method outperforms consistently the existing implementations, and implements high performance and low power gates that have a very large number of inputs. A new dual clocked design that uses memristors in current mode logic implementation of threshold logic gates is also presented. Memristor based designs have high potential to improve performance and energy over purely CMOS-based combinational methods. The proposed designs are clocked, and outperform a recently proposed combinational method in performance as well as energy consumption. It is experimentally verified that both designs scale well in both energy consumption as well as delay.

Introduction

Threshold gates operate on the majority or threshold decision principle, indicating that the output value is contingent upon whether the arithmetic total of its input values above a specified threshold. The threshold concept is inherently universal, with traditional logic gates like AND and OR serving as specific instances of threshold gates. Consequently, threshold logic can uniformly address both conventional gates and threshold gates. For several years, the design of logic circuits with threshold gates has been seen as an alternative to conventional logic gate design methodologies. The efficacy of the threshold gate design approach is in the inherent complicated functions executed by these gates, enabling system realizations that need fewer threshold gates or gate levels compared to designs

using regular logic gates. Recently, there has been a growing interest in threshold logic due to many theoretical studies demonstrating that polynomial-sized, bounded-level networks of threshold gates may perform functions that need unbounded-level networks of conventional logic gates. Significant operations such as multiple addition, multiplication, division, and sorting may be executed by polynomial-sized threshold circuits of limited constant depth. Threshold gate networks have been beneficial in modeling neural networks and brain architecture. With changeable threshold values, they have been used to simulate learning systems, adaptive systems, self-repairing systems, and pattern recognition systems, among others. The examination of strategies for synthesizing threshold gate networks is significant in fields like artificial neural networks and machine learning. Implementations of CMOS Threshold Gates The sufficiency of limit logic as a contemporary alternative The configuration of VLSI is determined by the availability, cost, and capabilities of the fundamental building blocks. Recently, many compelling circuit concepts have been explored to provide standard-CMOS ideal edge gates. The most promising are shown in this part. To denote their context of application, we distinguish between static and dynamic acceptance. Rationale for static edge doors: There are two notable approaches to static edge entryway CMOS implementations: one relies on the ganged technique, while the other employs the Neuron MOS (nMOS) transistor standard. Figure 1.1 illustrates the circuit configuration for these ganged-based transmission gates. Each information signal xi powers a ratioed CMOS inverter; all inverter outputs are hard-wired, producing a nonlinear voltage divider that drives a restoring inverter or a series of inverters. The technique for these gates involves measuring just two distinct inverters. Assuming uniform length for all transistors, the widths [Wp, Wn]i,b of each inverter are selected based on the wi and T values to be implemented. Weight values other than 1 may be accommodated by simply connecting in parallel the number of fundamental inverters (inverters with wi = 1) indicated by the weight value; conversely, the value of T is determined by the output inverter edge voltage. Due to the sensitivity of this voltage and Vf to process variations, the ganged-based TG has a limited fan-in. Nevertheless, the main drawback of this TG is its rather high power consumption.

Literature Survey

Analysis of Delays in Current Mode Threshold Logic Gate Designs. The current mode is a widely used CMOS-based realization of threshold logic functions, whereby the gate delay is contingent upon the sensor dimensions. This study introduces a novel implementation of current mode threshold functions aimed at enhancing gate delay and reducing switching energy. An analytical approach is presented to swiftly determine the sensor size that reduces gate latency. Simulation results for various gates using the optimal sensor size demonstrate that the proposed current mode implementation technique consistently surpasses previous implementations in terms of latency and switching energy. Minimal energy consumption, higher velocity, energy recuperation CMOS threshold logic gate A novel implementation of a threshold gate using a capacitive input and a charge recycling differential sense amplifier latch is introduced. Simulation findings demonstrate that the suggested structure exhibits minimal power dissipation and elevated operating speed, together with resilience to fluctuations in process, temperature, and supply

voltage, making it extremely appropriate for digital integrated circuit design. A low-power, high-performance threshold logic-based standard cell multiplier in 65 nm CMOS technology. This work details the design, simulation, manufacturing, and testing of a 32-bit 2's complement integer multiplier, created using a mix of CMOS standard cells and threshold logic components in a 65 nm low-power process. In comparison to a multiplier constructed only using CMOS standard cells, the threshold logic-based multiplier is 1.23 times smaller and uses 1.41 times less dynamic power and 2.5 times less leakage power at the same process corner. Current-Mode Threshold Logic Gates (CMTLG). Figure 2 illustrates a comprehensive circuit schematic of the CMTL gates. The low-swing inputs are sent to a PMOS-based CMTL gate. The CMTL gate detects low input variations, does logical operations, and generates full swing output voltages. The output nodes of the CMTL gate with full-swing serve as inputs to the nMOS-based interconnect driver. In the following section, we delineate current-mode threshold logic gates and introduce several implementations of these gates. A threshold gate is a superset of logic gates, including AND, NAND, OR, and NOR. It may be used to implement more complex functions, such as the majority function, inside a single logic gate. Figure 3 illustrates the fundamental functioning of the current-mode threshold logic gate. The PMOS transistor is used to convert the input voltage, which oscillates between VL and ground, into current. When the input at the gate terminal of the PMOS transistor is grounded, it may conduct a greater current than the PMOS transistor with a gate input voltage of VL. For minimal values of VL, the PMOS transistor is continuously activated. Implementations of a threshold logic function using CMTLG and DCML The nodes linking the differential section and the sensor section on the input side and the threshold side are M1 and M2, respectively. The sensor component has three p-MOS transistors (P1, P2, P3) and four n-MOS transistors (N1, N2, N3, N4), as seen in the image below. If the sensor size is S, then all p-MOS transistors in the sensor section measure S μm, whereas all n-MOS transistors in the sensor section measure less than S μm. The CMTLG's operation consists of two phases: the equalization phase and the assessment phase. The stages are elucidated with the assistance of Figures 1 and 5. When the applied clock (clk) to the CMTLG is high, the circuit enters the equalization phase. When the clock signal is low, the circuit enters the evaluation phase. During the equalization phase, transistors N1 and N2 are activated, resulting in nodes M1 and M2 exhibiting identical voltage levels due to transistor N1, while nodes O and OB maintain the same voltage due to transistor N2 (refer to Fig. 1). During the evaluation phase, transistors N1 and N2 are deactivated, and if the threshold current is inferior than the active current, the voltage at node O increases more rapidly than that at node OB. If, during the evaluation phase, the threshold current above the active current, the voltage at node OB increases more rapidly than that at node O. Figure 5 illustrates the two phases of the clock, the voltage at the output nodes O and OB, and the voltage differential between the output nodes O and OB (dV).

Proposed System Methodology

We examine an N-input CMTLG capable of executing various TLG functions for specified values of N and T. This section demonstrates how to determine the optimal size for the N-input CMTLG to minimize the latency of any TLG implemented by the N-input CMTLG. A novel TLG implementation is suggested. The term is Dual Clock based Current

Mode Logic (DCCML). The designation implies that two clocks are used to achieve low power consumption and high speed. The methodology has two phases. The functions that may be implemented using CMTLG for a certain input configuration (number of inputs N and threshold T) are categorized into analogous classes. We demonstrate that the TLG experiences its maximum latency when T+1 inputs are activated on the input side. Figure 3 illustrates the block diagram of DCCML. The differential block is subdivided into four components: the positive threshold, the negative inputs, the negative threshold, and the positive inputs. All transistors in the differential block are matched pMOS transistors linked in parallel, as seen in Fig. 3. The differential block has six pMOS transistors (P1 to P6) and three nMOS transistors (N1, N2, and N3). The gates of transistors P1 and N1 are linked to Clk1, whereas the gates of transistors P2, P5, and P6 are linked to Clk2. Transistor N1 functions as an equalizing transistor, balancing the voltage at nodes OP and OPB. Transistors P5 and P6 serve to isolate the differential block. The transistors at the positive and negative thresholds remain perpetually operational. The transistors in the positive and negative input blocks are activated based on the applied input pattern. The input pattern used for the positive inputs block is represented by {x1, x2, ..., xI}. Let N represent the total number of inputs, and I signify the quantity of positive inputs. The quantity of negative inputs is N minus I. The input pattern used for the negative inputs block is represented as {xI+1, xI+2, ..., xN}.

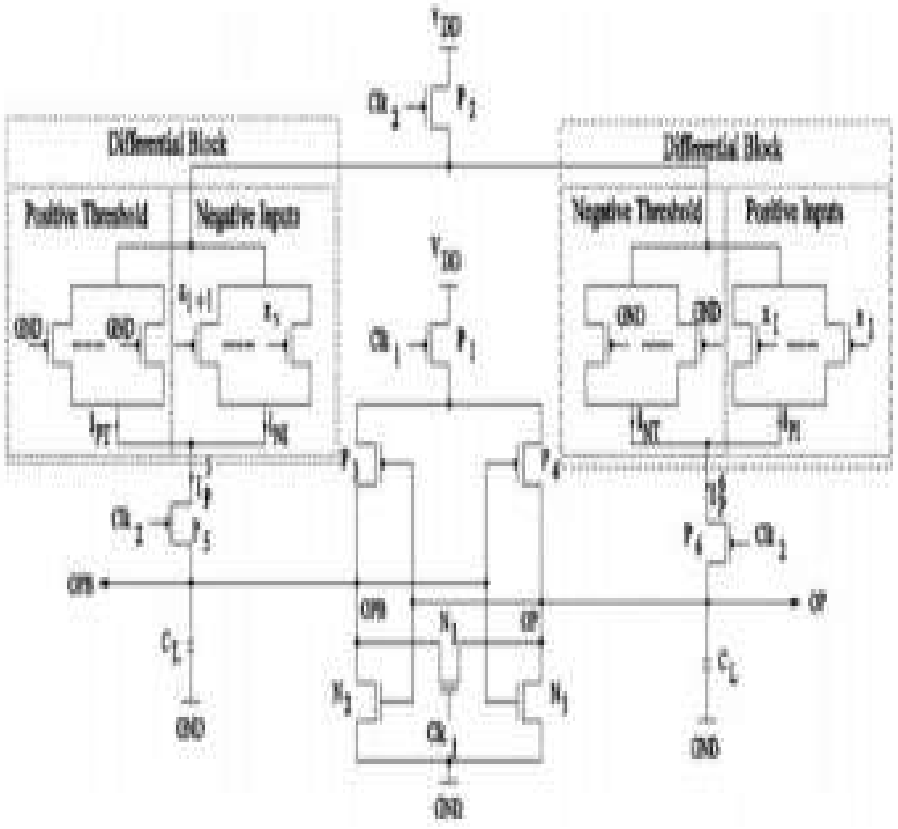

Fig.: Block diagram of DCCML TLG

Examine a function f, having a potential weight configuration {w1, w2: wT, w3, w4} = {2, 2:3, −1, −1}. In the specified weight arrangement, there exist two positive weights, w1 and w2, alongside two negative weights, w3 and w4. Weights w1 and w2 are applied to the positive input area, whereas weights w3 and w4 are applied to the negative input section. The threshold weight wT is applied in the positive threshold. The current traversing the four blocks (positive threshold, negative inputs, negative threshold, and positive inputs). Nodes OP and OPB serve as the output nodes. Load capacitance is represented by CL. The procedure consists of three phases: the equalization phase, the pre-assessment phase, and the final evaluation phase. When Clk1 and Clk2 are elevated, the circuit enters the equalization phase. When clocks Clk1 and Clk2 are low, the circuit is in the pre-evaluation phase. When Clk1 is low and Clk2 is high, the circuit is at the final assessment phase. It is seen that the functioning of the gate remains unaffected when the two clocks are not fully synchronized.

The CMTLG deferral may be categorized into two aspects: activation time and boosting time. The first viewpoint of the current mode limit rationale gate (CMTLG) pertains to the duration required to develop a little voltage differential (200 μV) between the nodes at Q and OP [2]. The intricacy between IA and IT, situated between hubs M1 and M2, induces a constant increase in voltage differential. To establish a fundamental voltage differential between the nodes Q and OP, the duration required by the CMTLG is referred to as the activation time TA. The activation time mostly shifts to the differential component. The second aspect is to reinforce the foundational voltage difference to a rational condition at the yield hubs, corresponding to the duration required by the sensor component. It is referred to as the boosting time TB. This TB mostly relies on the sensor component. The alternative solution involves the use of differential clock limit reasoning as detailed in [3], which is introduced as the differential current mode rationale approach. The piece graph is clearly seen in Fig. 3. It is further categorized into differential and sensor as CMTLG. IT refers to the current traversing the limit component, whereas IA denotes the current flowing through the information sources component. The sensor component consists of pMOS transistors labeled P1, P2, P3, P4, and nMOS transistors labeled N1, N2, N3, N4, N5, N6. The heap capacitance CL is coupled to both yield hubs Q and OP.

The applied clock is divided into two components: When the clock signal is high, the TLG is in the equilibrium phase, and when the clock signal is low (logic 0), it enters the evaluation phase. During the equalization step, the nMOS transistors N1, N2, N3, and N6 are in an active (ON) state. At nodes M1 and M2, the voltage across transistor N1 is equalized. At nodes M3 and M4, the transistor N2 stabilizes the voltage. During this phase, a discharge pathway for nodes Q and OP in Fig. 3 is present only when transistors N6 and N3 are activated. In the assessment phase, if a voltage discrepancy occurs at nodes Q and OP, the sensor component will detect the voltage difference and then adjust the output voltage to achieve a stable voltage level. The voltage at the yield hub Q increases more rapidly than at the hub OP, especially when the edge current IT is smaller than the dynamic current IA. At that juncture, low voltage is present at hub OP, whereas high voltage is associated with hub Q. When IA is smaller than IT, the voltage at OP increases more rapidly than the voltage at hub Q, resulting in a low voltage at OP. Figure 4 displays the two intervals of the check, illustrating the voltage difference

between hubs Q and OP (dV) as well as the voltage at Q and OP. In DCML, the two forms of delay are the activation time TA and the boosting time TB.

Result

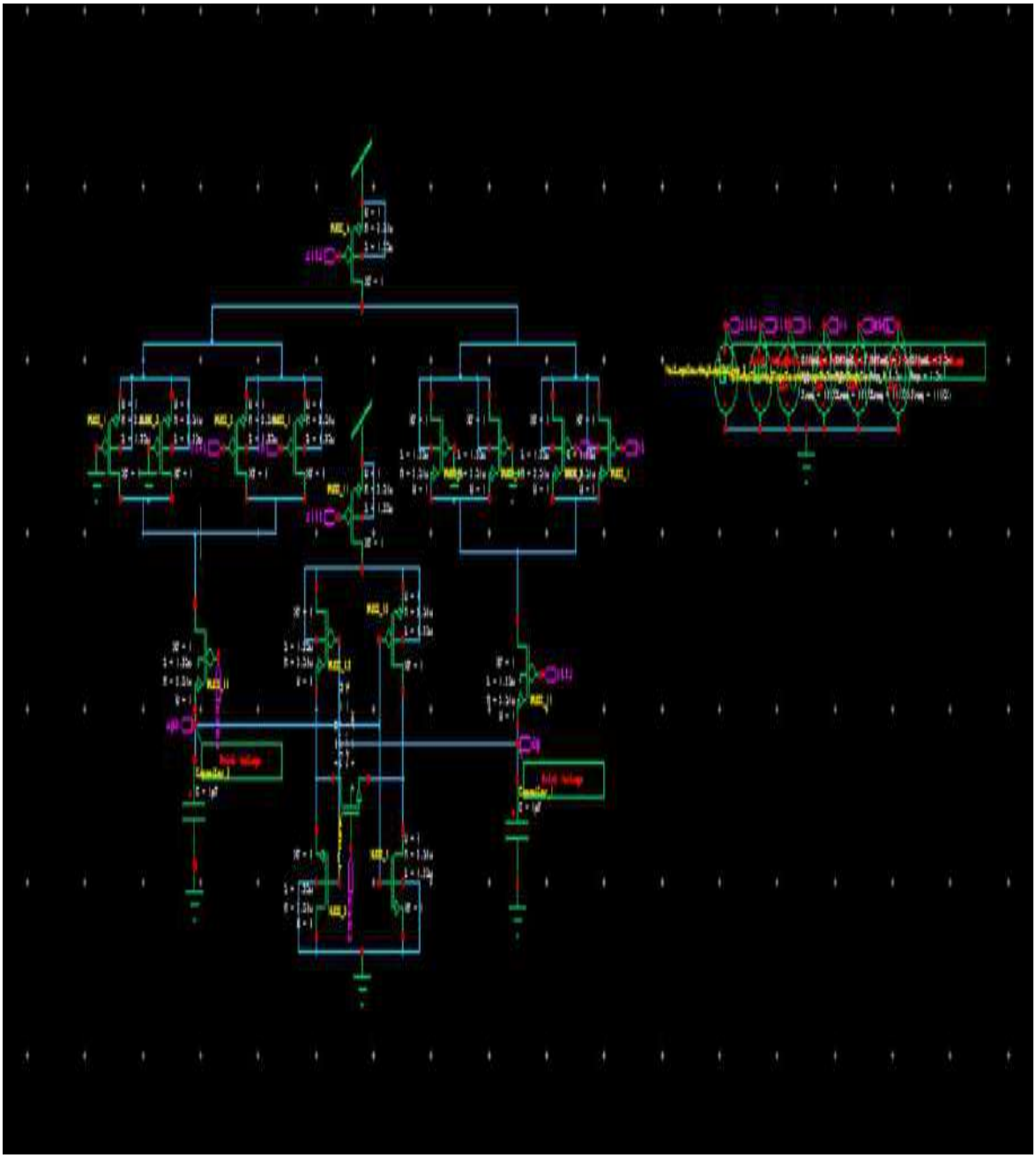

Fig: Schematic Diagram

Simulation results

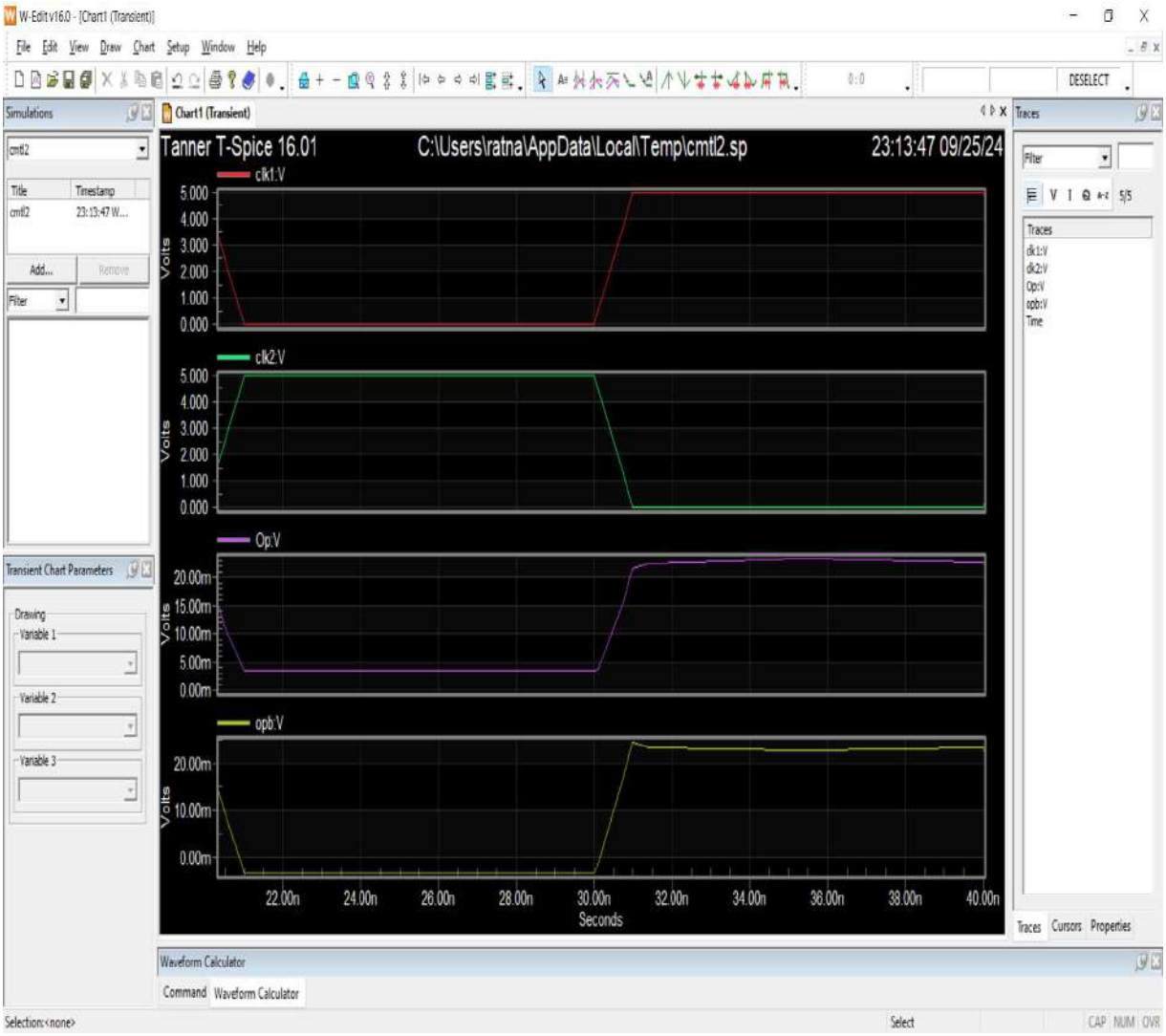

Fig: DCCML graph

Conclusion and Future Scope

A scientific method has been suggested to swiftly differentiate the transistor measurement in the sensor segment of a present mode application, ensuring minimal door delay (near the base), independent of the present mode approach used to perform the logical function. Another proposed execution methodology surpasses current methods in both latency and energy efficiency. Ultimately, the use of the aforementioned concepts results in decreased latency and enhanced noise immunity. The findings in the table clearly indicate that the suggested DCCML approach is applicable for designing high-speed and energy-efficient switching. Dual clock current mode threshold logic has been used in ultralow power applications, since research indicate that the current in typical static

CMOS circuits poses a significant difficulty in reducing energy dissipation. The dual clock current logic enables the attainment of both speed and switching energy efficiency.

Future scope

Threshold logic might be considered an alternative design methodology for digital circuits. This study developed a magnitude comparator by using threshold logic and the principles of resistive threshold logic in circuit implementation. The resistive threshold-based magnitude comparator yields results equivalent to those of the typical CMOS implementation, while offering improvements in transistor count and implementation area. The complexity of circuits designed using threshold logic is lower than that of traditional implementations. The importance of threshold logic is apparent in the execution of intricate circuits, as it facilitates a more efficient and cost-effective construction of such circuits. The concept of threshold logic may be expanded to facilitate the implementation of intricate circuits more effectively. This idea is appropriate for the systematic realization of complicated circuits and may be used in circuit design for efficient implementation. Consequently, the notion of threshold logic may serve as an alternate approach for the design and implementation of logic circuits.

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