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Design and Analysis of Approximate Multipliers using Approximate 4:2 Compressors

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Abstract

Approximate computing techniques have emerged as a promising approach to enhance efficiency by sacrificing a bit of accuracy. Within this framework, approximate multipliers have gained significant attention for their ability to find a sweet spot between precision, performance, and power efficiency. One popular method for creating these multipliers involves using 4:2 approximate compressors, which act as efficient components in approximate arithmetic circuits. This paper introduces two different designs for 4:2 approximate compressors, which are then utilized to deliberately decrease the accuracy of the multiplier while achieving substantial gains in power efficiency and speed. The effectiveness of these proposed designs has been confirmed through simulations using the Genus software, demonstrating a noteworthy 30% and 34% reduction in the required area and a 42% and 44% reduction in power consumption. Exact computing units aren't necessarily essential in applications like data mining and multimedia signal processing. They may be substituted with a similar item. Research into error tolerant applications using approximation computation is on the increase. These applications rely heavily on adders and multipliers. In digital signal processing, approximate complete adders are suggested at the transistor level. Partial product accumulation in multipliers is handled by their suggested full-adder design.

1-INTRODUCTION

Exact computing units aren't necessarily essential in applications like data mining and multimedia signal processing. They may be substituted with a similar item. Research into error tolerant applications using approximation computation is on the increase. These applications rely heavily on adders and multipliers. In digital signal processing, approximate complete adders are suggested at the transistor level. Partial product accumulation in multipliers is handled by their suggested full-adder design.

The use of truncation in fixed-width multiplication designs is common to simplify the circuitry. In order to compensate again for quantization error induced by the reduced portion, a variable correction component is added. Accumulation of bits is critical in terms pf power usage when using approximation methods in multipliers. If the least relevant bits of the inputs can be trimmed, then partial products may be formed in order to decrease hardware complexity. In partial product accumulations, the suggested multiplier saves just a few adder circuits. A partial product reduction trees of four 8 x 8Dadda multiplier variations is given and applied with two types of roughly 4-2 compressors. Mean relative error (MRE) is greatly affected by the suggested compressors in that they produce nonzero output for zero-valued inputs, which is a severe negative.

2-LITERATURE SURVEY

1. ” Approximate multiplier using approximate 4:2 compressors” (2023)- IEEE 20th India Council

International Conference (INDICON)

In contrast to accurate multipliers, these approximate multipliers display improved area utilisation, enhanced power efficiency, and reduced delay. Their capacity to achieve higher compression ratios and enhanced-computational efficiency positions approximate multipliers as a compelling solution for addressing the growing computational demands and enhancing performance across a spectrum of applications. Future progress in this field can be pursued through the refinement of approximate compression techniques and the quest for an optimal equilibrium between compression ratios and the accuracy of multiplication results.

2. Low-Power Approximate Multiplier-with Error Recovery using a New Approximate 4-2 Compressor," 2020- IEEE

A Low-Power Approximate Multiplier with Error Recovery using a New Approximate 4-2 Compressor is designed to balance power consumption, speed, and accuracy, particularly in applications where some level of error can be tolerated, such as image and signal processing. The 4-2 compressor is a crucial component in many multiplication processes. It is used to reduce the number of partial products generated during multiplication. The new approximate 4-2 compressor proposed in this approach is designed to further reduce power consumption by introducing minor computational errors that are rectified later in the pipeline.

3. Area Efficient Approximate 4–2 Compressor for Multiplier Design," 2020-IEEE India Council International Subsections Conference (INDISCON)

An area-efficient approximate 4–2 compressor is a hardware component used in digital circuit design, particularly in the design of multipliers. In digital multipliers, compressors are used to reduce the number of partial products during multiplication, thus speeding up the process and reducing power consumption. The 4–2 compressor takes four input bits and generates two output bits, which helps to consolidate data in arithmetic operations.

Approximate compressors differ from traditional ones in that they trade off accuracy for improvements in other parameters such as power consumption, area, and delay. The approximation is acceptable in many applications where absolute precision is not critical, such as in multimedia processing, machine learning, and signal processing.

3-Analysis of Approximate Multipliers using Approximate 4:2 Compressors

In modern applications, practicality often outweighs the pursuit of absolute precision. Hence, approximate computing has gained significant prominence, offering distinct advantages [1]. At the core of approximate arithmetic circuits, particularly in the context of approximate multipliers, resides the 4:2 approximate compressor. Its primary objective is to efficiently condense multiple input bits into a reduced set of output bits, consciously balancing precision against improvements in power efficiency and speed. The 4:2 approximate compressor transforms four input bits into two output bits, effectively compressing the input data. Unlike their precise counterparts that target exactness, approximate compressors deliberately introduce controlled errors to enable more efficient computations.

These errors are judiciously managed to minimize their impact while delivering substantial benefits in power and performance. Implementing 4:2 approximate compressors involves various approximation techniques, such as modified logic gates or simplified carry chains, intentionally introducing inaccuracies for more efficient

processing. Within multipliers, approximate compressors are pivotal, reducing precision while maintaining acceptable performance standards . They enable a tradeoff, allowing controlled inaccuracy in exchange for enhanced power efficiency, reduced area, and faster operation.

The applicability of 4:2 approximate compressors extend beyond multipliers to domains like digital signal processing, error-tolerant applications, machine learning, and image and video processing. In these contexts, where some error resilience is acceptable, approximate compressors significantly improve computational efficiency, leading to reduced power consumption and enhanced system performance.

Block Diagram

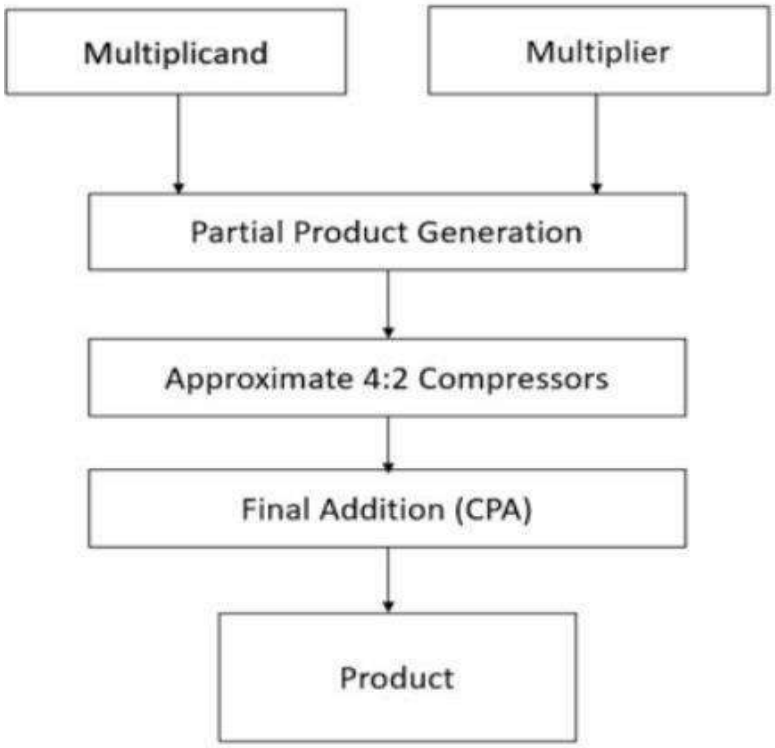


Fig:2.4 Block Diagram f Approximate Multipliers using Approximate 4:2 Compressors

Methodology

The methodology for designing and analyzing approximate multipliers using approximate 4:2 compressors involves several key steps. First, a thorough literature review is conducted to understand existing techniques in approximate multiplication and the role of compressors.

Next, the design begins with the generation of partial products using standard AND gates to facilitate the multiplication of input binary numbers. These partial products are then processed through approximate 4:2 compressors, which reduce four input bits to two output bits along with a carry, introducing an intentional approximation to enhance speed and reduce complexity.

The compressed outputs are subsequently summed using an approximate adder, allowing for further optimization of speed and power

consumption. To analyze the performance of the design, simulations are run using software tools such as ModelSim or Cadence, focusing on metrics such as latency, power consumption, area utilization, and accuracy. The results are then compared with traditional exact multipliers to evaluate trade-offs between performance and precision. Finally, an error analysis is conducted to quantify the accuracy loss, ensuring that the approximate multipliermeets the requirements for its intended applications. This structured methodology aims to provide a comprehensive understanding of the benefits and limitations of using approximate 4:2 compressors in multiplier designs.

4-SOFTWARE REQUIREMENTS

The software must facilitate efficient processing of posit numbers, incorporating error handling and optimization techniques to enhance computational speed and accuracy. Additionally, requirements for performance monitoring and power management features are essential to align with the project's objectives of minimizing energy consumption. Clear and well-defined software requirements not only guide developers in creating robust applications but also help in managing expectations among stakeholders, ultimately leading to the successful delivery of a product that meets its intended purpose in an efficient and effective manner.

XILINX Software

Xilinx Tools is a suite of software tools used for the design of digital circuits Implemented using Xilinx Field Programmable Gate Array (FPGA) or Complex Programmable Logic Device (CPLD). The design procedure consists of (a) design entry, (b) synthesis and implementation of the design, (c) functional simulation and (d) testing and verification. Digital designs can be entered in various ways using the above CAD tools The CAD tools enable you to design combinational and sequential circuits starting with VHDL HDL design specifications. The steps of this design procedure are listed below:

- Create VHDL design input file(s) using template driven editor.
- Compile and implement the VHDL design file(s).
- Create the test-vectors and simulate the design (functional simulation) without using a PLD (FPGA or CPLD).
- Assign input/output pins to implement the design on a target device. Download bit stream to an FPGA or CPLD device.

Creating a New Project

Xilinx Tools can be started by clicking on the Project Navigator Icon on the Windows desktop. This should open up the Project Navigator window on your screen. This window shows the last accessed project.

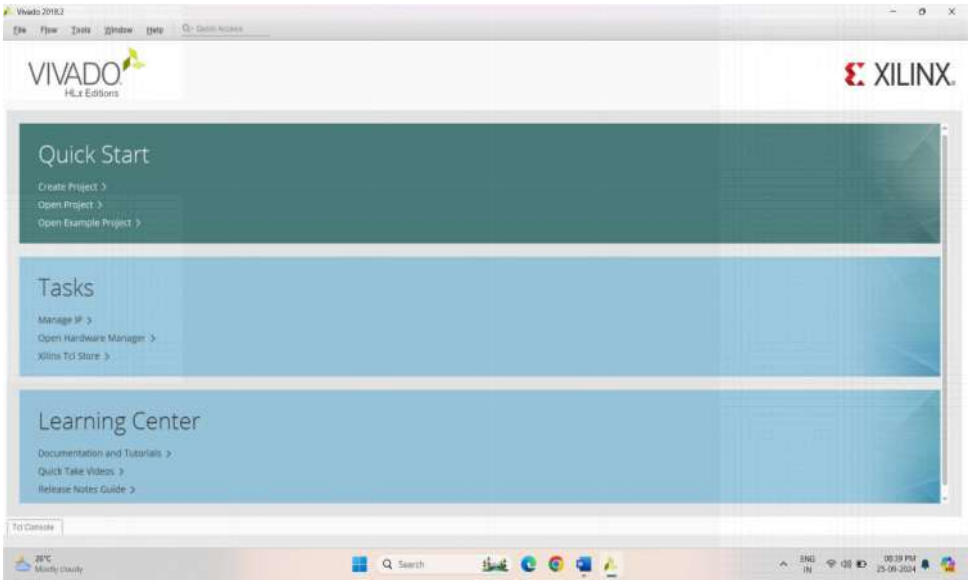


Fig 3.2.1: Vivado Project Navigator window (snapshot from vivado software)

5-ADVANTAGES, DISADVANTAGES AND APPLICATIONS

Advantages

Approximate multipliers using approximate 4:2 compressors offer several advantages, especially in applications where precise results are not mandatory, such as image processing, signal processing, and machine learning. Here are 15 key advantages of using approximate multipliers with approximate 4:2 compressors:

Reduced Power Consumption: Approximate multipliers consume less power due to the simplification in logic circuits, making them ideal for low-power devices and applications.

- Lower Area Requirements: Approximate 4:2 compressors reduce the number of transistors and gates needed, leading to a smaller chip area, allowing more components to fit on a single chip.
- Increased Speed: With fewer logic gates and simplified operations, the critical path is shorter, leading to faster computation times and higher performance.
- Lower Latency: Approximate designs have reduced computation delays, making them suitable for real-time applications where quick processing is required.

Disadvantages

Approximate multipliers using approximate 4:2 compressors come with certain tradeoffs that may not be suitable for every application. Here are 10 key disadvantages:

- Loss of Accuracy: The most significant drawback is the intentional loss of accuracy, which may not be acceptable for applications Error Propagation: Errors in approximate multipliers can propagate through successive computational stages, leading to cumulative inaccuracies that affect the final results.
- Unpredictable Behaviour in Critical Systems: In systems where precise operations are critical, such as control systems or safety-critical applications, the uncertainty introduced by approximate designs can result in unpredictable or unsafe outcomes.
- Limited Application Scope: Approximate multipliers are unsuitable for applications requiring exact computations, such as encryption, data

compression, and error correction, which rely on accurate arithmetic operations.

Applications

The design and analysis of approximate multipliers using approximate 4:2 compressors is an emerging area of interest in approximate computing. Approximate computing techniques tradeoff accuracy for power, performance, and area (PPA) improvements, which is beneficial in error-tolerant applications such as multimedia, machine learning, and signal processing. Here are some key applications:

Image and Video Processing

Image Compression: In lossy image compression algorithms like JPEG, exact computations are not necessary, as the human eye cannot perceive small errors. Approximate multipliers using approximate 4:2 compressors can speed up operations such as Discrete Cosine Transform (DCT) while reducing power consumption.

Video Encoding/Decoding: Approximate arithmetic units are beneficial in video encoding algorithms (like H.264 or H.265) where some error tolerance is permissible without significant degradation in visual quality.

Machine Learning and AI

Neural Networks: Many machine learning models, particularly neural networks, can tolerate approximate arithmetic operations due to their inherent error resilience. Approximate multipliers using 4:2 compressors can speed up computations such as matrix multiplication in deep learning models, leading to faster training and inference times while saving energy.

Inference Engines: In edge computing devices for real-time AI inference, low-power approximate multipliers are valuable in reducing power consumption without significant accuracy loss.

6-RESULT AND SIMULATION

Approximate multipliers using approximate 4:2 compressors aim to enhance performance metrics such as power consumption, speed, and area at the expense of reduced accuracy. The approximate 4:2 compressor simplifies the logic used for accumulation by modifying the sum and carry logic, which reduces the number of transistors and the overall complexity of the circuit. This approach significantly lowers power consumption and propagation delay compared to exact compressors. When applied to multipliers, the use of these approximate compressors helps reduce the critical path, improving speed and energy efficiency. However, the accuracy loss must be carefully analyzed to ensure that it remains acceptable for the intended application, particularly in fields like image processing or machine learning, where slight inaccuracies may not heavily impact overall system performance.

Simulations of approximate multipliers show improved power savings and reduced delay, often with marginal degradation in output quality. The results indicate that power consumption and area are reduced by up to 30%–50% depending on the design, while delay is reduced by 20%– 40%. However, the introduced error in multiplication results varies, often expressed as error metrics like Mean Relative Error Distance (MRED) or normalized mean square error (NMSE). These errors tend to be application-specific, with tolerable levels depending on the use case. For example, in multimedia applications, the human eye might not perceive minor errors in the output, making the trade-off highly effective.

RTL And Technology Schematics

RTL (Register Transfer Level) diagram for a specific circuit or system, possibly related to SecureBallot Lite. The diagram illustrates the flow of data and control signals through various components,

including inverters, adders, multiplexers, comparators, and other logic gates. The inputs, represented by y[7:0], are processed through these components to produce the output, represented by z[7:0]. However, without more context, it is difficult to determine the exact functionality of the circuit.

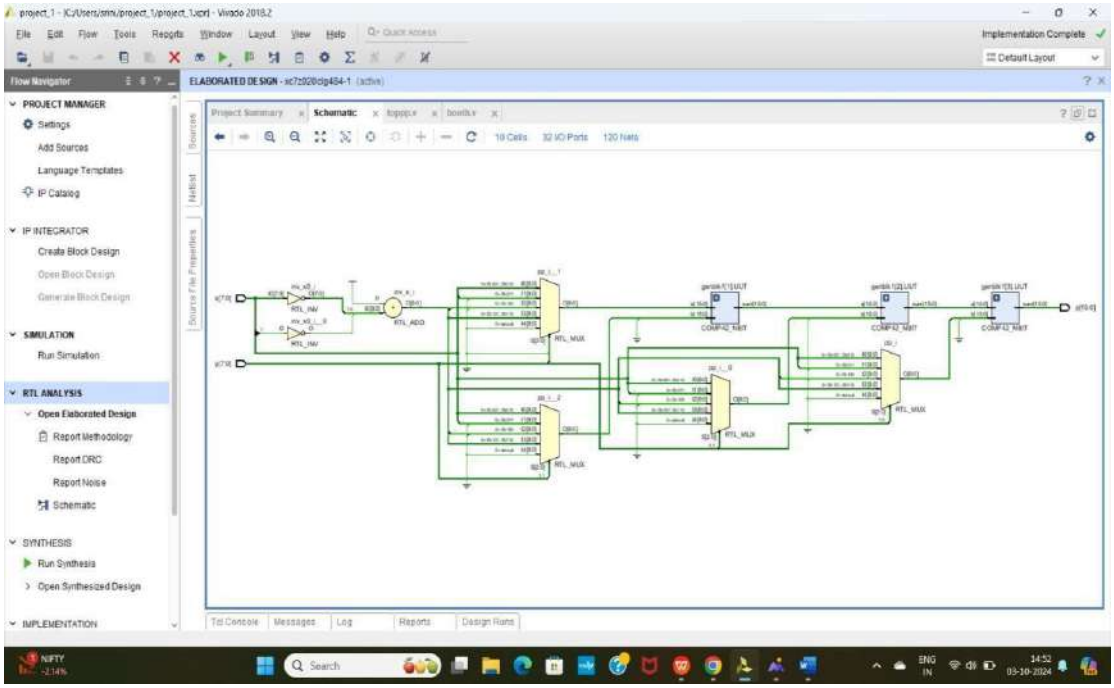
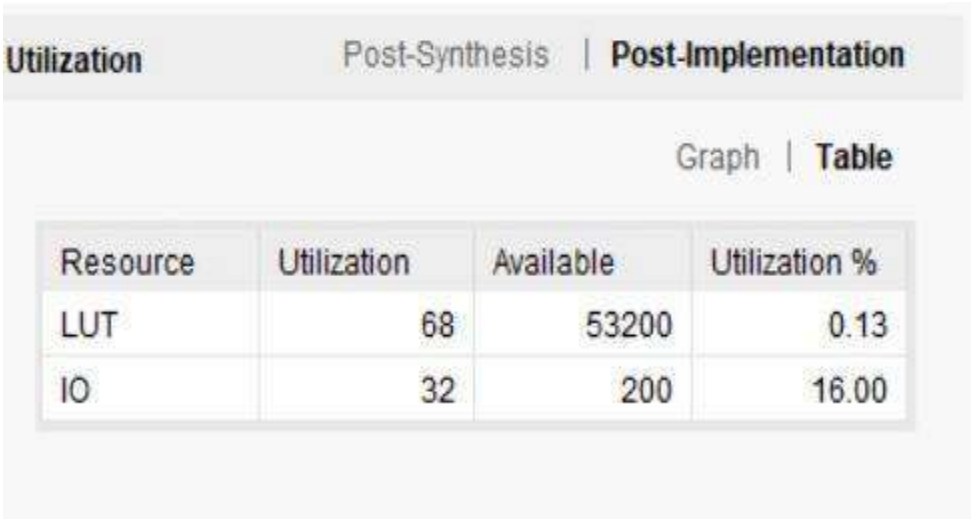


Fig 4.2: RTL Diagram of Approximate Multipliers

Area



Resource	Utilization	Available	Utilization %
LUT	68	53200	0.13
IO	32	200	16.00

Fig 4.3.1: Synthesis result of Area

LUTs: The design is using 68 out of 53200 available LUTs, which is a very low utilization of 0.13%. This suggests that the design is small and simple, and there's plenty of room for additional logic.

IOs: The design is using 32 out of 200 available IOs, which is a moderate utilization of 16.00%. This means that a significant portion of the available IOs are being used, and there might be constraints on adding more external

connections. 4.3.2 Delay

```
Timing Report

Slack:                  inf
  Source:               y[3]
                          (input port)
  Destination:          p[15]
                          (output port)
  Path Group:           (none)
  Path Type:            Max at Slow Process Corner
  Data Path Delay:      15.843ns  (logic 6.091ns (38.447%)  route 9.752ns (61.553%))
  Logic Levels:         11  (IBUF=1 LUT3=1 LUT4=2 LUT5=5 LUT6=1 OBUF=1)
```

Fig 4.3.2 Synthesis result of Delay

15.843ns: This is the total propagation delay of the path, consisting of logic delay (6.091ns) and routing delay (9.752ns).logic 6.091ns (38.447%): This indicates that the logic elements contribute 38.447% to the total delay.route 9.752ns (61.553%): This indicates that the routing wires contribute 61.553% to the total delay. the timing report indicates that the design meets all timing constraints and has a total propagation delay of 15.843ns. The majority of the delay is contributed by the routing wires, which suggests that optimizing the routing could potentially improve the performance.

Power

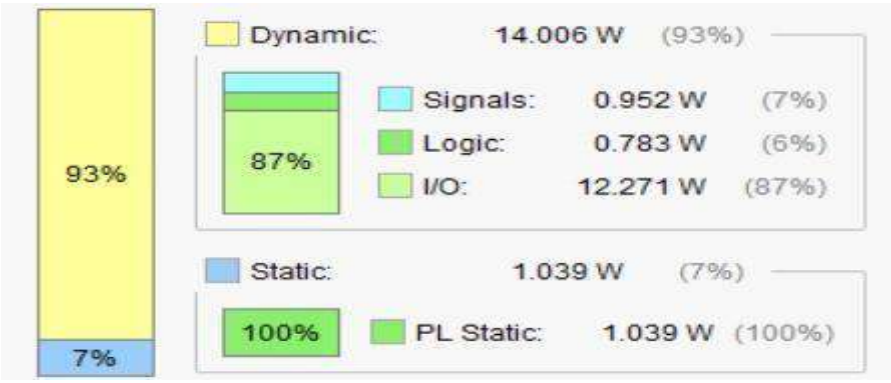


Fig 4.3.3 Synthesis result of power

Dynamic Power: This is the power consumed when the device is actively processed or performing tasks. It's typically higher than static power.

Static Power: This is the power consumed even when the device is idle or not performing any tasks. It's consumed statically, even when the device is idle. often referred to as "leakage" power. The device or system is consuming a total of 15.045 W, with the majority of the power (93%) being consumed dynamically while processing data or performing tasks. The remaining 7% is

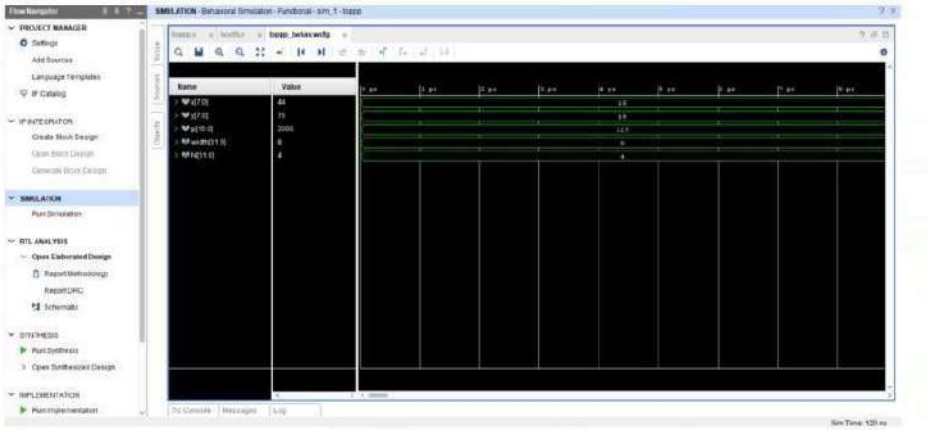


Fig 4.3.4 Simulation result of approximate multiplier using approximate 4:2 compressors (A Snapshot from Vivado Software)

	Area (µm2)	Power(W)	Dela y (ns)
Accurate 4:2 compressor	39.4	$9.01x10^{-7}$	659
Existing approximate 4:2 compressor-1	34.8	$1.07x10^{-6}$	381
Existing approximate 4:2 compressor-2	27.2	$8.45x10^{-6}$	314
Approximate 4:2 compressor-1	23.5	$6.34x10^{-7}$	276
Approximate 4:2 compressor-2	21.9	$6.19x10^{-5}$	307

Table 2: Synthesis Report of 4:2 Compressors

Table 2 provides a comprehensive overview of the synthesis reports for various compressors, accentuating the performance of the approximate designs in comparison to their precise counterparts. When juxtaposed with the accurate compressor-1, the approximate compressors manifest noteworthy reductions in the area, achieving a reduction of 32% and 36%, respectively, and realising area savings of 14% and 19% when contrasted with the approximate compressor-2. Additionally, with regards to power consumption, they outperform accurate compressor-1, resulting in a substantial 40% and 42% reduction in power usage, while exhibiting a remarkable 92% decrease when compared to approximate compressor-2. Moreover, the approximate compressors exhibit enhanced delay characteristics, reducing delay by 27% and 19% in comparison to accurate compressor-1 and showcasing a 12% and 2% delay improvement over approximate compressor-2.

7-CONCLUSION

In conclusion, the design and analysis of approximate multipliers using approximate 4:2 compressors present a promising approach to reducing power consumption, area, and delay in arithmetic circuits. By introducing small errors in computations, these approximate compressors strike a balance between computational accuracy and resource efficiency, making them ideal for applications in error-resilient domains such as image processing, machine learning, and signal

processing. While the trade-offs in precision can be carefully controlled, the overall performance improvement in terms of speed and energy efficiency makes this technique a valuable contribution to the development of low-power, high-performance systems. Further exploration of errortolerant applications and optimization techniques can lead to even more refined designs in future work.

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