ISSN 2277-2685
IJESR/June. 2025/ Vol-15/Issue-3s/770-778
B.HemaSri *et. al.,* / International Journal of Engineering & Science Research

A Partially Static High Frequency 18T Hybrid Topological Flip Flop Design for Low Power Application

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ABSTRACT

An extremely low power true 1 φ clocking flip-flop is proposed using eighteen transistors only. The flip-flop is a synchronous bistable element that stores single-bit information. To design this Master Slave (MS) type architecture, topological, logical, and adaptive coupling techniques are employed. The minimum number of transistors are maintained by using above techniques, which comprises of complementary pass transistor logic and static complementary MOS logic. It also offers low power, a low delay that speeds up the flip-flops, and low complexity by reducing the transistor count. The proposed circuit is implemented using Cadence Virtuoso and compared with the five other reported logic structures of flip-flops. This project proposes a novel 18-transistor (18T) hybrid topological flip-flop design tailored for low-power, high-frequency applications. By integrating partially static and dynamic circuit techniques, the flip-flop achieves enhanced power efficiency and reduced switching activities. The architecture employs a mix of static storage and dynamic clock gating to minimize power consumption during idle states, making it suitable for modern high-performance systems-on-chip (SoCs) operating in energy-constrained environments. This hybrid design is ideal for systems requiring both high-speed operations and low-energy footprints, making it highly applicable to portable and IoT devices.

1-INTRODUCTION

In electronics, a flip-flop or latch is a circuit that has two stable states and can be used to store state information. A flip-flop is a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems. Flip-flops and latches are used as data storage elements. A flip-flop stores a single bit (binary digit) of data; one of its two states represents a "one" and the other represents a "zero". Such data storage can be used for storage of state, and such a circuit is described as sequential logic. When used in a finite- state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs). It can also be used for counting of pulses, and for synchronizing variably timed input signals to some reference timing signal. Flip- flops can be either simple (transparent or opaque) or clocked (synchronous or edge- triggered). Although the term flip-flop has historically referred generically to both simple and clocked circuits, in modern usage it is common to reserve the term flip-flop exclusively for discussing clocked circuits; the simple ones are commonly called latches.

Early flip-flops were known variously as trigger circuits or multivibrators. According to P.

L. Lindley, an engineer at the US Jet Propulsion

Laboratory, the flip-flop types detailed below (SR, D, T, JK) were first discussed in a 1954 UCLA course on computer design by Montgomery Phister, and then appeared in his book Logical Design of Digital Computers.[9][10] Lindley was at the time working at Hughes Aircraft under Eldred Nelson, who had coined the term JK for a flip-flop whch changed states when both inputs were on (a logical "one"). The other names were coined by Phister. They differ slightly from some of the definitions given below. Lindley explains that he heard the story of the

JK flip-flop from Eldred Nelson, who is responsible for coining the term while working at Hughes Aircraft. Flip flops are an application of logic gates. With the help of Boolean logic, you can create memory with them. Flip flops can also be considered as the most basic idea of a Random Access Memory [RAM]. When a certain input value is given to them, they will be remembered and executed, if the logic gates are designed correctly. A higher application of flip flops is helpful in designing better electronic circuits. The most used application of flip flops is in the implementation of a feedback circuit. As a memory relies on the feedback concept, flip flops can be used to design it. There are mainly four types of flip flops that are used in electronic circuits. They are:

- The basic Flip Flop or S-R Flip Flop
- Delay Flip Flop [D Flip Flop]
- J-K Flip Flop

2- LITERATURE SURVEY

The Literature Survey for the project "A Partially Static High Frequency 18T Hybrid Topological Flip-Flop Design for Low Power Application" explores key areas in consumption. Flip- flops are essential building blocks in digital systems, used for data storage and synchronization. Traditional flip-flops, such as the 6-transistor (6T) design, are simple but face challenges in achieving high performance while maintaining low power consumption. This motivates the search for more advanced flip-flop designs that strike a balance between these two requirements. Low power consumption has become increasingly critical with the rise of portable, battery-powered devices. As a result, various techniques like clock gating, dual- threshold CMOS, and voltage scaling have been developed to reduce both dynamic and static power dissipation. However, these methods often conflict with the need for higher speeds, which is why high-speed flip-flops utilizing dynamic logic have been introduced. Dynamic logic allows for faster switching but often leads to higher power consumption, creating a trade-off between speed and energy efficiency. To address these issues, hybrid flip-flop designs that combine static and dynamic logic have gained attention. Static logic provides stability and noise immunity, while dynamic logic enhances speed, allowing for faster transitions and lower power consumption. The 18T flip-flop design represents an advanced approach where more transistors improve stability and reduce race conditions, enhancing performance. However, this additional complexity requires careful design to avoid excessive power consumption.

Low-power techniques such as adiabatic logic and pass-transistor logic have been explored to further reduce energy dissipation in CMOS-based circuits. Integrating these with hybrid flip- flop designs can lead to a significant reduction in power while maintaining high-speed operation. Furthermore, research comparing the performance of traditional flip-flops with more advanced hybrid designs has

demonstrated improvements in speed, power efficiency, and stability, making them ideal for high-performance digital

systems. Recent advancements in CMOS technology, including sub-threshold operation and the use of fin FETs, open new opportunities for further optimizing flip-flop designs. Machine learning techniques and optimization algorithms are also being explored to enhance the design process, enabling more efficient, compact, and power-efficient flip- flops for future digital applications. The literature suggests that hybrid flip-flop designs, such as the 18T design, can meet the growing demands for high-speed and low-power performance in modern digital circuits.

3-A PARTIALLY STATIC HIGH FREQUENCY 18T HYBRID TOPOLOGICAL FLIP FLOP DESIGN FOR LOW POWER APPLICATION

Design and Implementation

Existing systems related to the Partially Static High Frequency 18T Hybrid Topological Flip- Flop Design for Low Power Application largely consist of conventional flip-flop designs, including static, dynamic, and hybrid flip-flops, each offering a specific balance between performance, power consumption, and stability.

Traditional flip-flops, such as the 6-transistor (6T) design, are widely used due to their simplicity and reliability. While they are suitable for many applications, they face limitations in terms of speed and power efficiency, particularly in high-frequency operations. As the clock speed increases, the power dissipation of 6T flip-flops rises, making them less ideal for modern low-power, high-performance applications. Their relatively high static and dynamic power consumption, especially in circuits operating at higher frequencies, necessitates the need for more advanced designs.

Dynamic flip-flops, which use dynamic logic, offer faster switching times and are designed to meet the speed requirements of modern high-frequency circuits. However, while dynamic flip- flops achieve speed, they suffer from several drawbacks, including lower stability, greater susceptibility to noise, and higher power dissipation over time. Their performance can degrade in certain conditions, leading to increased complexity and challenges in maintaining reliability. These limitations make dynamic flip-flops less suitable for low-power applications that demand both performance and stability.

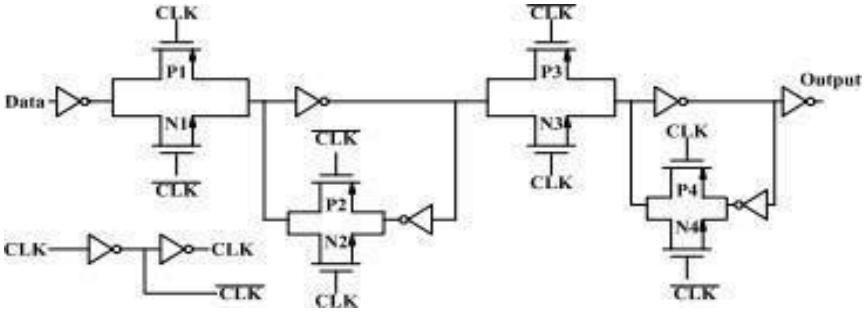

Figure- 3.1: Schematic of Existing circuit

In this section, the design is based on Transmission gate Logic. The flip-flop designed is of master-slave flip-flop. The block diagram for this conventional design is as shown below. It faces certain issues including-

- High Power Consumption.
- More Transistor Count.
- Performance is slow.

Proposed System

For achieving lower delay, decreasing the circuit complexity and optimizing the power consumption, we have topologically and logically reduced the number of the transistor especially PMOS transistor. Due to the low mobility of the PMOS transistors, we have reduced the continuous 2 PMOS (i.e., in ACFF) transistors in the same path from VDD to GND. This leads to reduction in delay of the proposed flip-flop. Moreover, the proposed design consumes lesser area as compared to LRFF, due to low circuit complexity. Figure 3.2 shows our proposed design, named as a Hybrid flip-flop (HFF). Since, it comprises logic reduction and balance clock as well.

The proposed hybrid structure consists of both LRFF and ACFF that meet the requirements by using only 18 transistors. The hybrid topological structure consists of 4 pass transistors (P2, P3, N6 and N7), two NMOS to hold data in master transistors and 6 inverters. Among the four pass transistors, one pair of pass transistors behaves as an auxiliary transistor (AT) to deliver weak 0 or Strong 1. Other pair of pass transistor behaves as a current booster (CB). A. Data Latching Cases:

1) Case (Data 0 and Clock 0): When CLK 0 and DATA 0, P1, P2, and N4 transistors will be in ON state, that makes node “u1” to be equal to 1. But “master” node and node u2 will not deliver any data to slave latch, because transistors N6 and N7 are OFF. Hence slave will hold its previous value at the output node. In this condition transistor P3, behaves as an AT since it passes weak 0 at the “master” node. The transistor P2, behaves as current booster because it passes strong 1 that conforms the logic 0 at master node.

2) Case (Data 0 and Clock 1): When CLK 1 and DATA 0, transistors N6 and N7 will be in ON state. The data stored at the “master” node and node u2, feeds to slave nodes “a” and “b”, via N6 and N7 respectively. This provides the data at the output through the slave. When master node output is 0, N6 is a CB, as it passes strong “0” at node “a”. At the same time N7 is an AT, as it passes weak “1” at node “b”. 3) Case (Data 1 and Clock 0): When CLK 0 and DATA 1, transistors N1, P2 and P4 will be in ON condition. That pulls node u1 and u2 to logic “0”, while master node retains the data at logic “1”. The slave will hold its previous value at the output node. In this condition transistor P2, behaves as an AT, as it passes weak 0 at node u1.

3) Whereas transistor P3, behaves as a CB, as it passes strong 1 at master node. 4) Case (Data 1 and Clock 1): When CLK 1 and DATA 1 logic at the master node will be transferred to slave similar to the above case as CLK 1. When the master node output is at logic “1”, N7 behaves as a CB, as it passes strong “0” at node “b”. At the same time N6, behaves as an AT, as it passes weak “1” at node “a”.

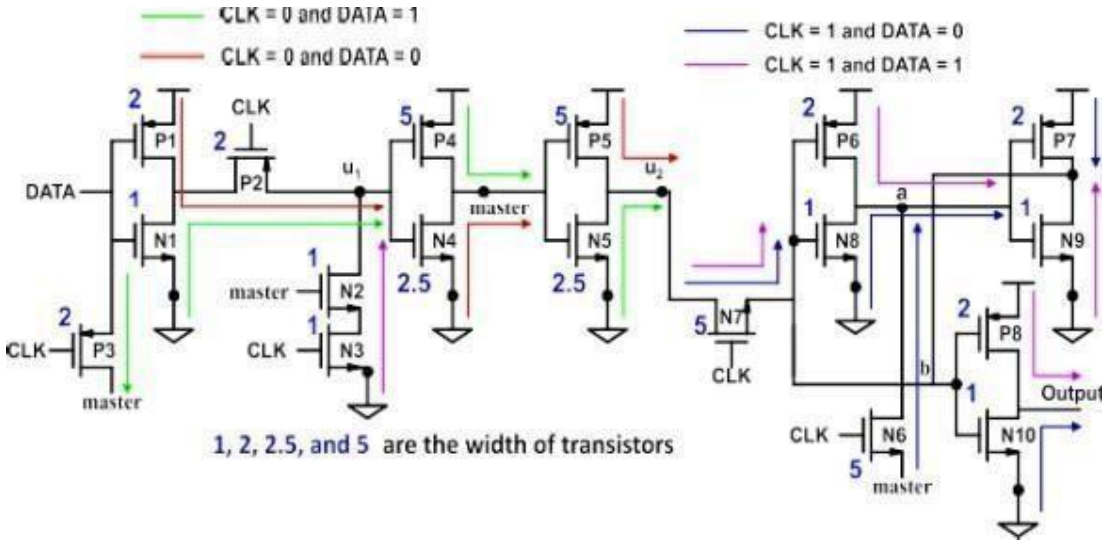

Figure-3.2. CMOS circuit of proposed work.

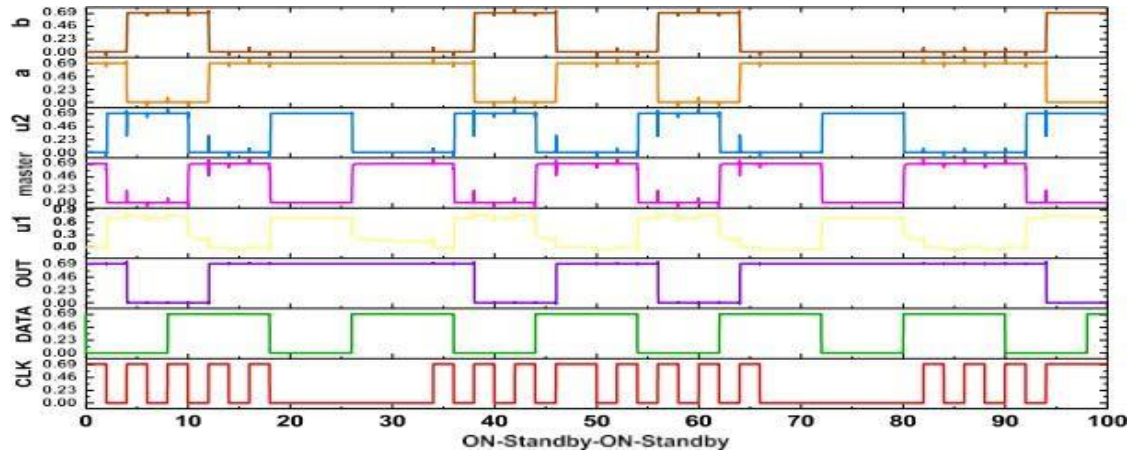

Figure-3.3 Running condition of HFF in the ON-STAND-ON mode in random data and clock input with clock frequency 250MHZ at 0.7V

Figure 3.3 indicates internal node voltages of the proposed Hybrid flip-flop, in which all nodes are static except node u1. The node voltage of u1 introduces small fluctuations but, logic remains at the same level hence circuit is partially static. The maximum peak of glitch at node u2 is 12.58% while voltage required to turn on the next transistor is 43.71%. This is too higher than the peak glitch value. So, these glitches will not affect flip-flop operation. To compensate these fluctuations, transistors P4/N4 and P5/N5 have aspect ratio of 5W/2.5W. All the nodes are providing rail to rail swing. The rise time of the CLK and Data is taken as 10 ps for static timing analysis. The change in output is occurring at every rising edge of the clock pulse. The output node, “a”, and “b” are always static.

The clock signal is suspended perpetually, when it is in the standby mode. This work is a partially static flip-flop; it might undergo in voltage deterioration in the standby mode because of floating node in the

circuit. Recommencing of clock signal is the wakeup mode and loading of flip-flop with entirely a new input data. So that, the flip-flop can restart its operation instantly and employ in any logic transitions immediately after restarting the clock signal. There is no need of signal recovery time to restart its operation.

To validate the claim, a simulation setup is created for input data. This simulation process starts with five clock cycles normally. Afterwards, six clock cycles for a standby mode, and the clock signal is recommenced again for a fresh input data setting. The simulated output waveforms are depicted in Figure 3.3. The proposed Hybrid flip-flop has been simulating at a supply voltage of 0.7 V.

4-RESULTS

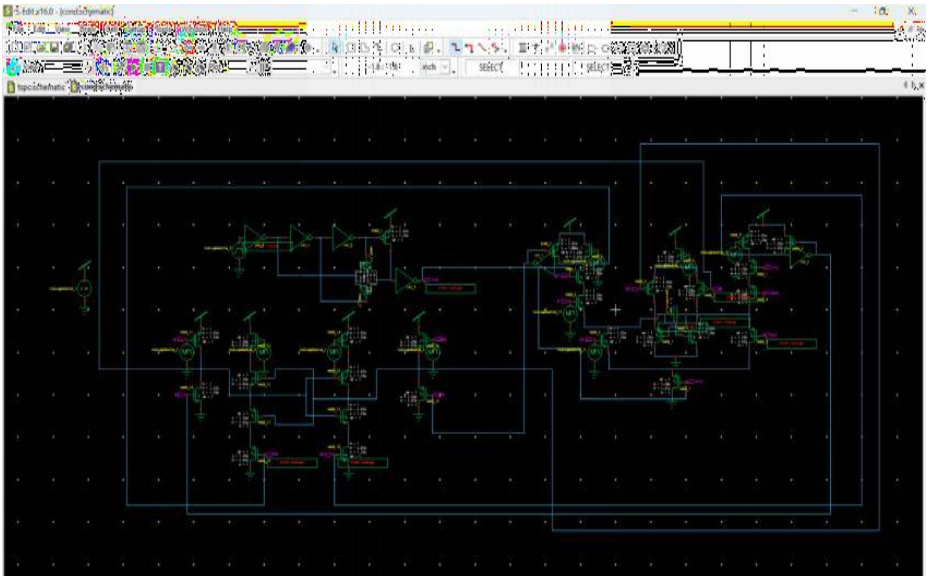

Figure-1: Schematic Diagram of Existing System

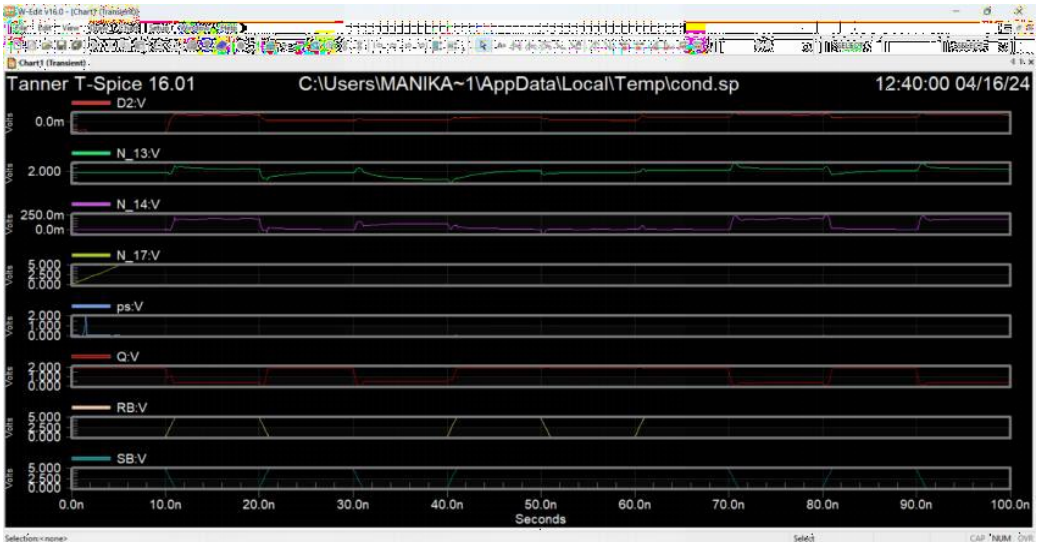

Figure-2: Waveform Of Existing System

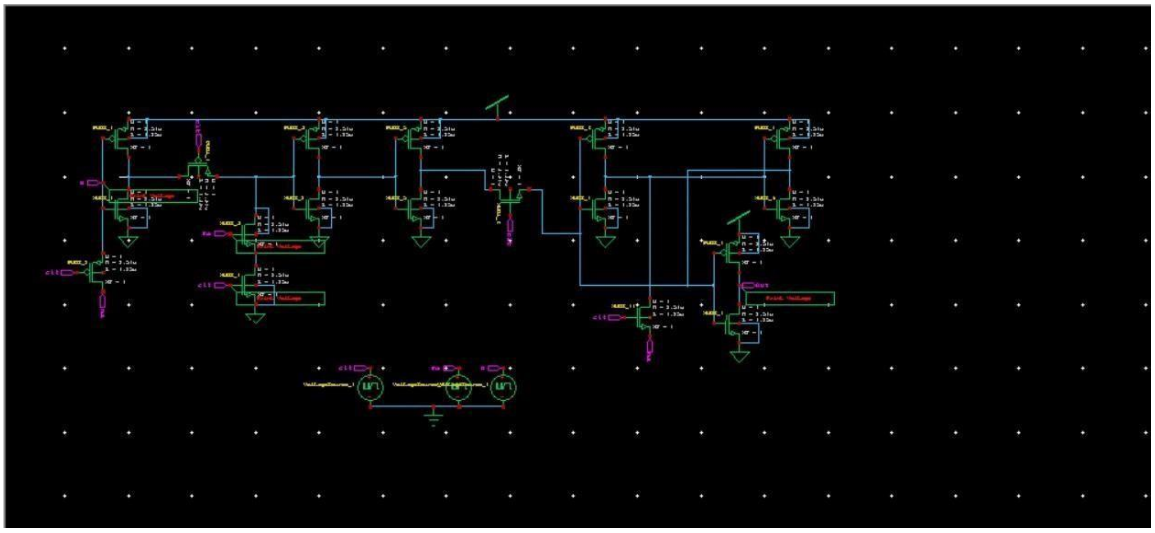

Figure- 3: Simulation Result of Phase 1

Figure- 4: Waveform results of Phase 1

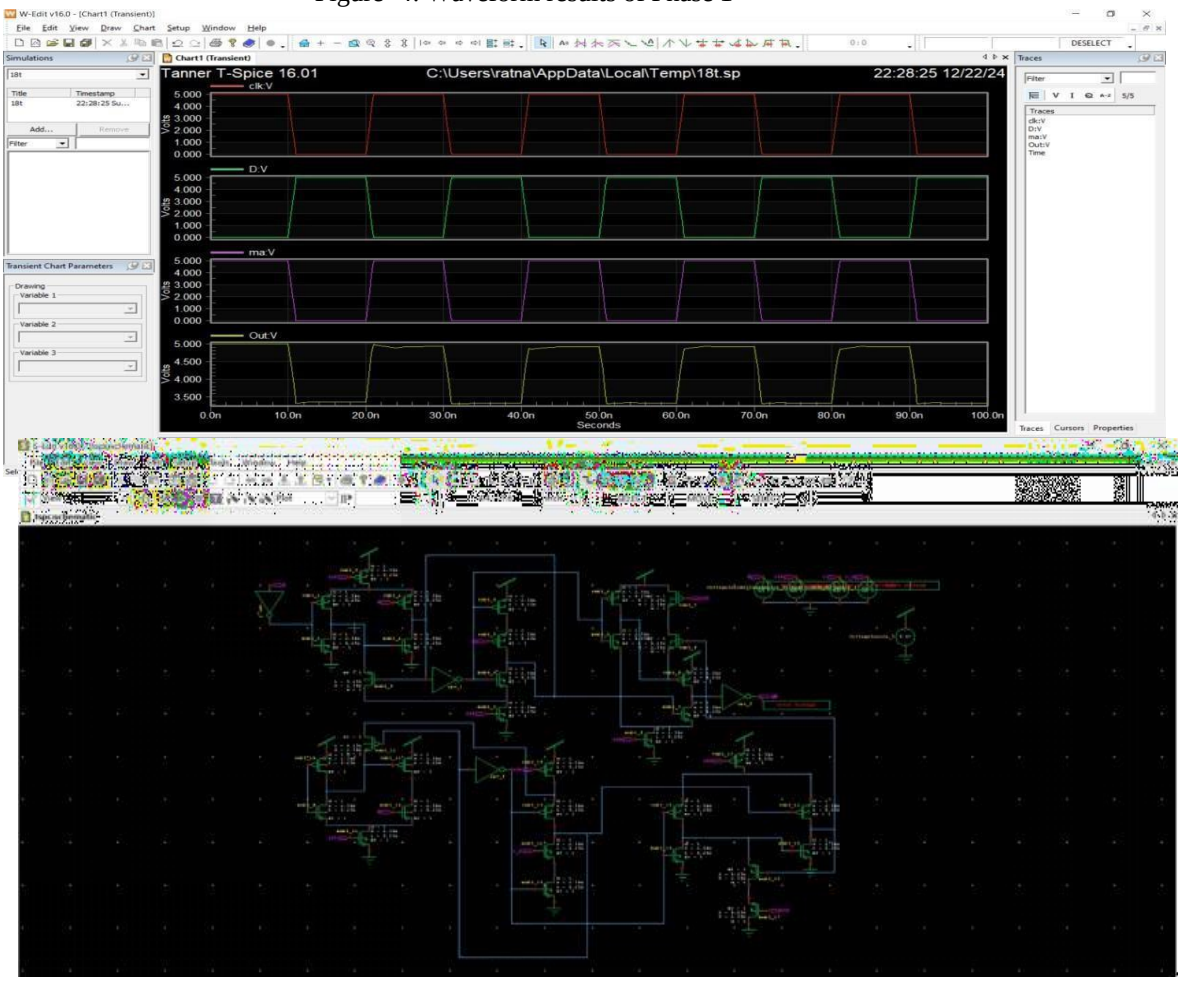

Figure-5: Schematic Diagram of of Phase 2

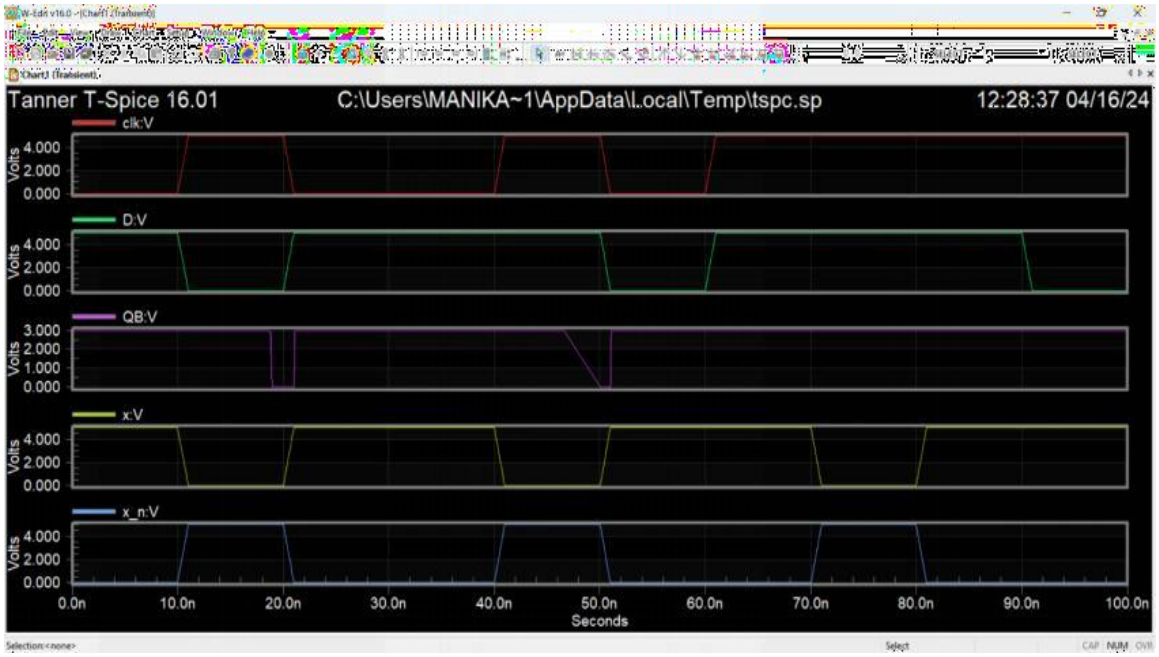

Figure- 7: Waveform Of Phase 2

5-CONCLUSION

A new flip-flop is designed by using 18 transistors. For the proposed work, we have considered following parameters, which are C to Q delay, reduction in PMOS transistor count, no clock overloading, and lowering circuit complexity. The proposed circuit outperformed by 52.52%, 62.89%, and 49.73% in terms of power consumption as compared to ACFF, TCFF and LRFF respectively. In terms of leakage power our circuit excelled by 4.20%, 19.27% and 39.75% when compared with ACFF, TCFF, and LRFF respectively. It also excels in performance at different supply voltages, frequency range and does not have clock overloading. All the parameters taken for this work have been successfully addressed. The proposed design is also compared with the 18T TSPC FF. In which we are getting comparable results, and, in some comparison, proposed circuit excels over 18T TSPC and hence proves the efficiency.

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