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Full Length Article

An Analytical Study Of High-Speed Low-Power Decoder Circuits Employing Mixed Logic

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Abstract
This research introduces an innovative design methodology for line decoders based on a hybrid logic framework. The proposed approach strategically integrates transmission gate logic, dual-value pass transistor logic, and conventional static CMOS logic to achieve an optimal balance between performance, power efficiency, and area utilization. For the 2-to-4 decoder, two distinct configurations have been developed: A 14-transistor design optimized for minimal transistor count and reduced power consumption. A 15-transistor design focused on superior power-delay product performance.
Each of these configurations supports both fixed-function and adaptive operating modes, resulting in four unique decoder variants. Furthermore, four new 4-to-16 decoder architectures have been realized by combining the proposed 2-to-4 pre-decoder stages with traditional CMOS-based post-decoder logic. Compared to conventional CMOS implementations, the suggested decoders demonstrate notable advantages, including higher output voltage swing and a reduced overall transistor count. Comprehensive simulations performed using a 32 nm technology node confirm significant improvements in both power consumption and propagation delay characteristics. The hybrid logic strategy presented in this work offers a promising direction for designing high-performance, energy-efficient decoders suitable for modern VLSI applications where speed, power, and reliability are critical design constraints.

Keywords: *Hybrid Logic Design, Line Decoder, Transmission Gate Logic, Pass Transistor Dual-Value Logic, Static CMOS Logic.*

Introduction To Vlsi

VLSI stays for "Generous Scale Integration". This is the field which incorporates squeezing progressively justification devices into smaller and more diminutive regions. VLSI, circuits that would have devoured boardfuls of room would now have the capacity to be put into a little space couple of millimeters over! This has opened up a noteworthy opportunity to do things that were improbable beforehand. VLSI circuits are everywhere .your PC, your auto, your new out of the plastic new best in class modernized camera, the cell phones, and what have you. This incorporates a lot of expertise on various fronts inside a comparative field, which we will look at in later portions. VLSI has been around for a long time, yet as a response of advances in the domain of PCs, there has been a passionate extension of contraptions that can be used to diagram VLSI circuits. Close by, conforming to Moore's law, the limit of an IC has extended exponentially consistently, to the extent computation control, utilization of available domain, yield. The combined effect of these two advances is that people would now have the capacity to put diverse helpfulness into the IC's, opening up new unsettled areas. Models are introduced structures, where smart devices are put inside normal things, and ubiquitous handling where small enrolling contraptions increase to such an extent, to the point that even the shoes you wear may truly achieve something supportive like checking your heartbeats. Facilitated circuit (IC) development is the engaging advancement for a whole host of creative devices and structures that have changed the way in which we live. Jack Kilby and Robert Noyce got the 2000 Nobel Prize in Physics for their production of the joined circuit; without the organized circuit, neither transistors nor PCs would be as basic as they are today. VLSI systems are extensively humbler and exhaust less power than the discrete sections used to build electronic structures beforehand the 1960s. Blend empowers us to fabricate structures with various more transistors, empowering essentially all the more enrolling ability to be associated with dealing with an issue.

Composed circuits are furthermore considerably less requesting to plan and make and are more reliable than discrete systems; that makes it possible to make exceptional reason structures that are more viable than comprehensively helpful PCs for the activity that should be finished.

Decoders

STATIC cmos circuits are used for most by a long shot of basis doors in fused circuits They involve complemen-tary N - type metal-oxide-semiconductor (nMOS) pulldown and P-type metal-oxide semiconductor (pMOS) pullup frameworks and present incredible execution and also security from confusion and contraption assortment. Thusly, essential metal-oxide semiconductor (CMOS) method of reasoning is depicted by quality against voltage scaling and transistor estimating and thusly tried and true assignment at low voltages and little transistor sizes [2]. Data signals are related with transistor entryways simply, offering decreased diagram versatile quality and help of cell-based method of reasoning mix and plan.

Pass transistor reason (PTL) was basically made in the 1990s, when diverse diagram styles were familiar pointing with give an appropriate differentiating alternative to CMOS justification and im-show speed, power, and region. Its rule layout differentiate is that data sources are associated with both the gateways and the source/exhaust diffu-sion terminals of transistors. Line decoders are basic circuits, for the most part used as a piece of the periphery equipment of memory displays (e.g., SRAM). This short develops a mixed method of reasoning procedure for their execution, picking improved execution appeared differently in relation to single-style layout. Whatever is left of this brief is dealt with as takes after: Section II gives a short survey of the assessed decoder circuits, realized with consistent CMOS reason. Portion III in-troduces the new mixed method of reasoning blueprints. Zone IV drives a close multiplication look at among the proposed and con-ventional decoders, with a point by point chat on the surmised comes to fruition. Fragment V gives the blueprint and last completes of the work presented.

Table I
Truth Table Of The 2–4 Decoder

A	B	D_0	D_1	D_2	D_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Table 2
Truth Table Of The Inverting 2–4 Decoder

A	B	I_0	I_1	I_2	I_3
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

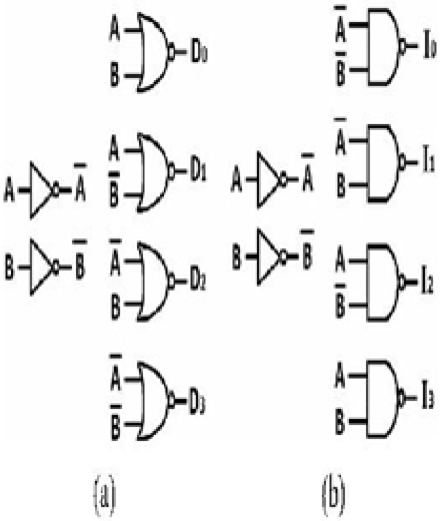
Overview Of Line Decoder Circuits

In advanced frameworks, discrete amounts of data are repre-sented by twofold codes. A n-bit parallel code can speak to up to 2n particular components of coded information. A decoder is a combina-tional circuit that proselytes parallel data from n input lines to a most extreme of 2n remarkable yield lines or less if the n-bit coded data has unused blends. **2– 4 Line Decoder**

A 2– 4 line decoder creates the 4 minterms D0−3 of 2 input factors An and B. Its method of reasoning movement is dense in Table I. Dependent upon the data mix, one of the 4 yields is picked and set to 1, while the others are set to 0. A changing 2– 4 decoder makes the fundamental minterms I0−3, consequently the picked yield is set to 0 and the rest are set to 1, as showed up in Table II. In conventional CMOS blueprint, NAND and NOR entryways are needed to AND or conceivably, since they can be realized with 4 transistors, rather than 6, likewise executing justification limits with higher adequacy. A 2– 4 decoder can be completed with 2 inverters and 4 NOR passages Fig. 1(a), while a changing decoder requires 2 inverters and 4 NAND entryways Fig. 1(b), both yielding 20 transistors.

B. 4– 16 Line Decoder With 2– 4 Predecoders

A 4– 16 line decoder delivers the 16 minterms D0−15 of 4input elements A, B, C, and D, and a switching 4– 16 line decoder creates the equal minterms I0−15. Such circuits can be completed using a predecoding procedure, as shown by which bits of n address bits can be predecoded into 1-of-2n predecoded lines that fill in as commitments to the last stage decoder [1]. Thusly, a 4– 16 decoder can be imple-mented with 2 2– 4 modifying decoders and 16 2-input NOR portals [Fig. 2(a)], and a changing one can be executed with 2 2– 4 decoders and 16 2-input NAND passages [Fig. 2(b)]. In CMOS method of reasoning, these layouts require 8 inverters and 24 2-input entryways, yielding an entirety of 104 transistors each



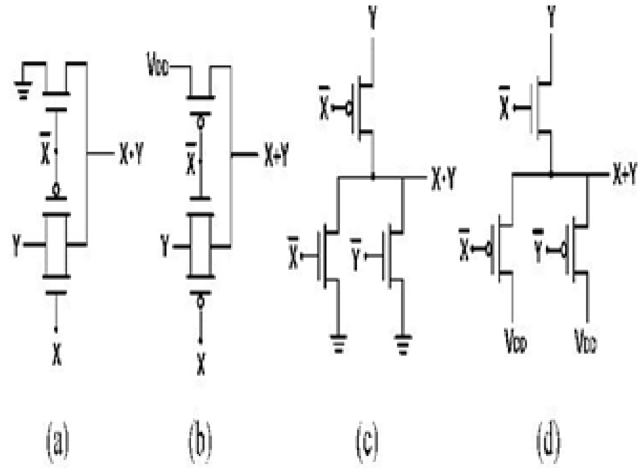


Fig :1. 20-transistor 2–4line decoders implemented with CMOS logic. (a) Noninverting NOR-based decoder. (b) Inverting NAND-based decoder

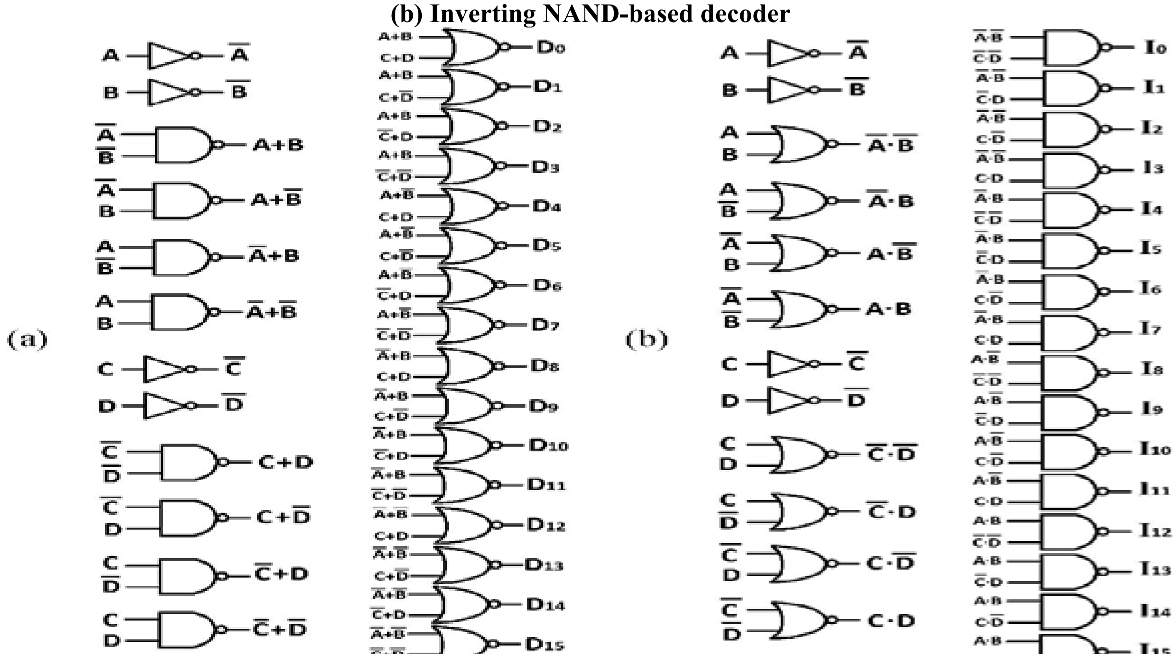


Fig. 2. 104-transistor 4–16 line decoders implemented with CMOS logic and predecoding.

(a) Noninverting decoder implemented with two 2–4 inverting predecoders and a NOR-based postdecoder. (b) Inverting decoder implemented with two 2–4 noninverting predecoders and a NAND-based postdecoderA. 14-Transistor 2– 4 Low-Power Topology

Planning a 2– 4 line decoder with either TGL or DVL entryways would require an aggregate of 16 transistors (12 for AND/OR doors and 4 for inverters). Be that as it may, by blending both AND door composes into a similar topology and utilizing appropriate flag course of action, it is conceivable to dispose of one of the two inverters, in this manner diminishing the aggregate transistor tally to 14.

Give us a chance to accept that, out of the two data sources, in particular, An and B, we intend to wipe out the B inverter from the circuit. At long last, The D3 minterm (AB) is executed with a TGL door, hence, the B inverter can be wiped out from the circuit, bringing about a 14-transistor topology (9 nMOS and 5 pMOS).

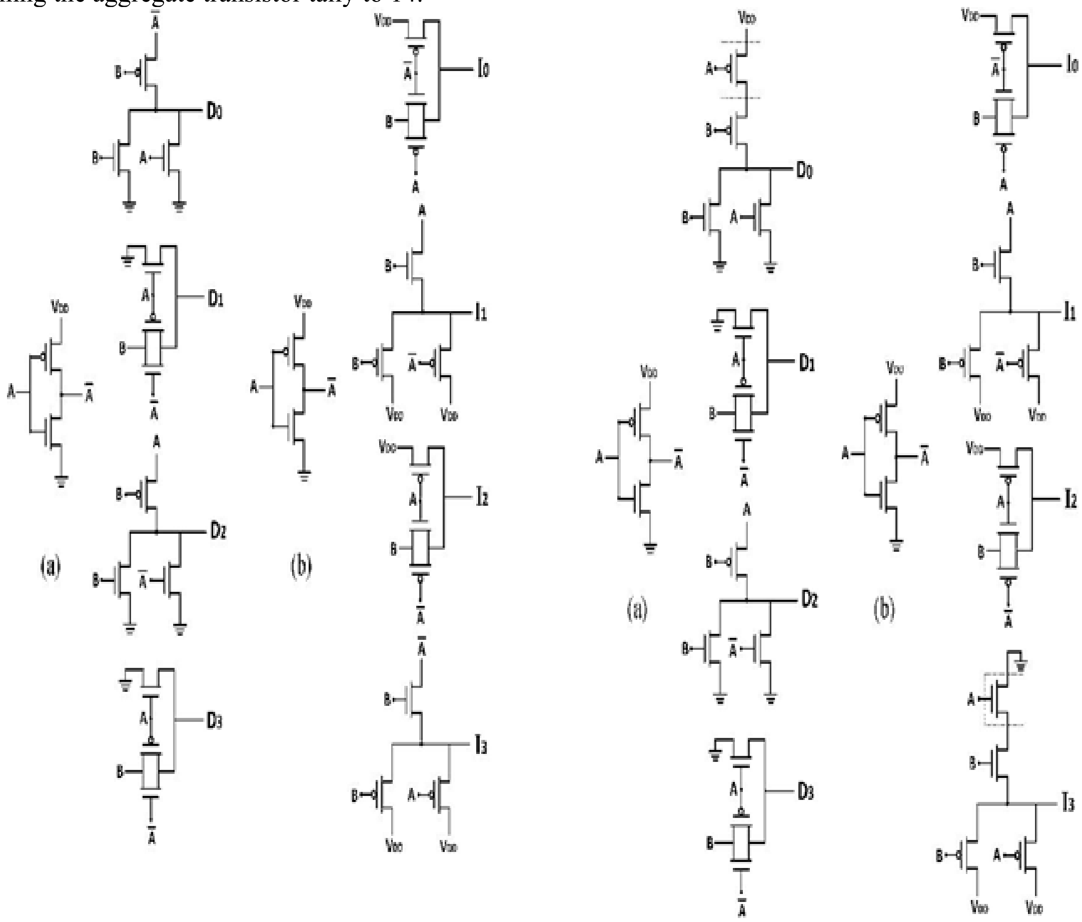


Fig. 3. New 14-transistor 2–4 line decoders. (a) 2–4LP. (b) 2–4LPI.

Following a comparable strategy with OR entryways, a 2– 4 reversing line decoder can be actualized with 14 transistors (5 nMOS and 9 pMOS) also: I0 and I2 are executed with TGL (us-ing B as the proliferate flag), and I1 and I3 are executed with DVL (utilizing An as the engender flag). The B inverter can by and by be omitted.

Inverter end lessens the transistor check, intelligent exertion and by and large exchanging action of the circuits, in this way diminishing force dispersal. The two new topologies are named "2– 4LP" and "2– 4LPI," where "LP" remains for "low power" and "I" for "altering." Their schematics are appeared in Fig. 4(a) and (b), individually.

B. 15-Transistor 2– 4 High-Performance Topology

The low-control topologies exhibited above have a downside in regards to most pessimistic scenario delay, which originates from the utilization of correlative An as the spread flag on account of D0 and I3. Notwithstanding, D0 and I3 can be productively actualized utilizing static CMOS doors, without utilizing integral sig-nals. In particular, D0 can be actualized with a CMOS NOR door and I3 with a CMOS NAND entryway, adding one transistor to every topology. The new 15T outlines present a huge change in delay while just marginally expanding power dissemination. They are named "2– 4HP" (9 nMOS, 6 pMOS) and "2– 4HPI" (6 nMOS, 9 pMOS), where "HP" remains for "superior" and "I" remains for "transforming." The 2– 4HP and 2– 4HPI

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schematics are appeared in Fig. 5(a) and (b), separately.

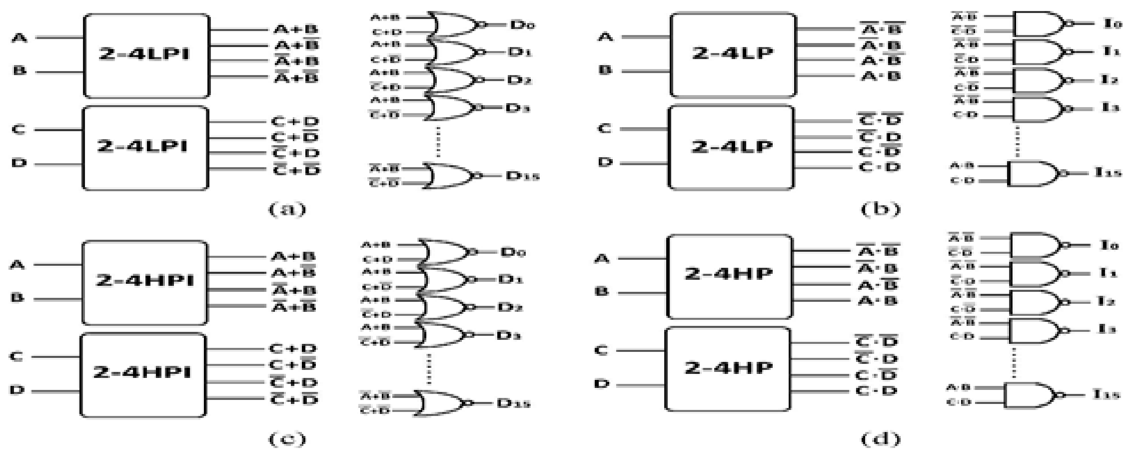


Fig.4. New 4–16 line decoders. (a) 4–16LP. (b) 4–16LPI. (c) 4–16HP. (d) 4–16HPI

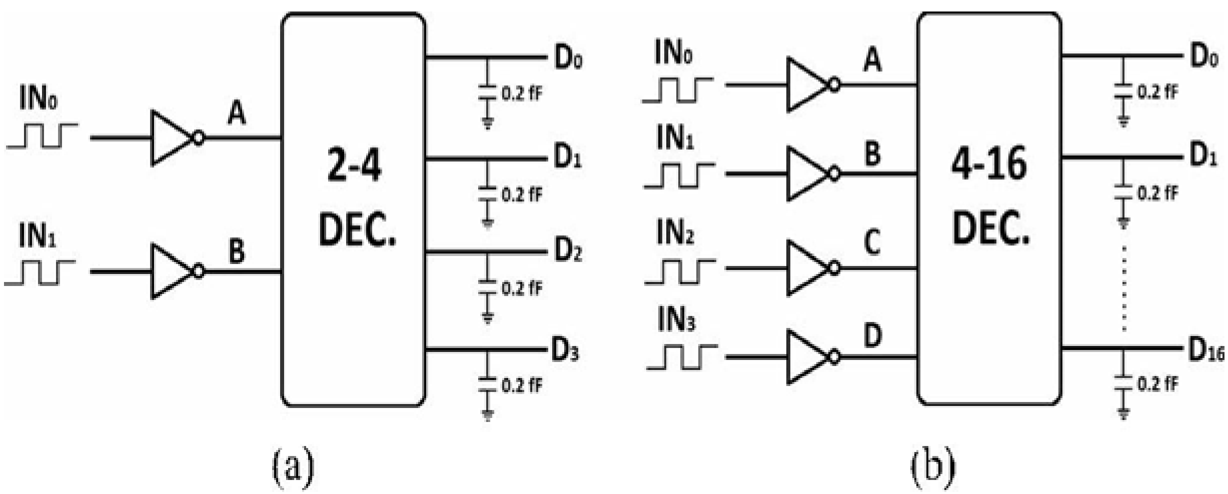


Fig. 5. Simulation setup regarding input/output loading conditions. (a) 2–4 de-coders. (b) 4–16 decoder

Simulations

In this area, we play out an assortment of BSIM4-construct flavor recreations in light of the schematic level, keeping in mind the end goal to contrast the proposed blended rationale decoders and the ordinary CMOS. The circuits are actualized utilizing a 32 nm prescient tech-nology display for low-control applications (PTM LP), incor-porating high-k/metal door and stress impact [11]. For reasonable and fair-minded examination we utilize unit-measure transistors solely (Ln = Lp = 32 nm, Wn = Wp = 64 nm) for all decoders.

A. Recreation Setup

All circuits are recreated with fluctuating recurrence (0.5, 1.0, 2.0 GHz) and voltage (0.8, 1.0, 1.2 V), for a sum of 9 reenactments. Every reproduction is rehashed 5 times with shifting temperature (−50, −25, 0, 25, and 50 ◦C) and the normal power/delay is ascertained and exhibited for each situation. All in-puts are cushioned with adjusted inverters (Ln = Lp = 32 nm, Wn = 64 nm, Wp = 128 nm) and all yields are stacked with a capacitance of 0.2 fF, as appeared.

Moreover, legitimate piece arrangements are embedded to the in-puts, keeping in mind the end goal to cover every conceivable progress a decoder can perform. A 2– 4 decoder has 2 inputs, which can create 22 = 4 distinctive twofold blends, in this manner yielding an aggregate of 4 ∗ 4 = 16 conceivable changes. The 2– 4 decoders are reproduced for 64 nanoseconds (ns), with the goal that the 16-bit input successions are rehashed 4 times. Also, a 4– 16 decoder has 4 inputs, 42 = 16 input blends and 16 ∗ 16 = 256 conceivable advances, in this manner the 4– 16 decoders are reproduced for

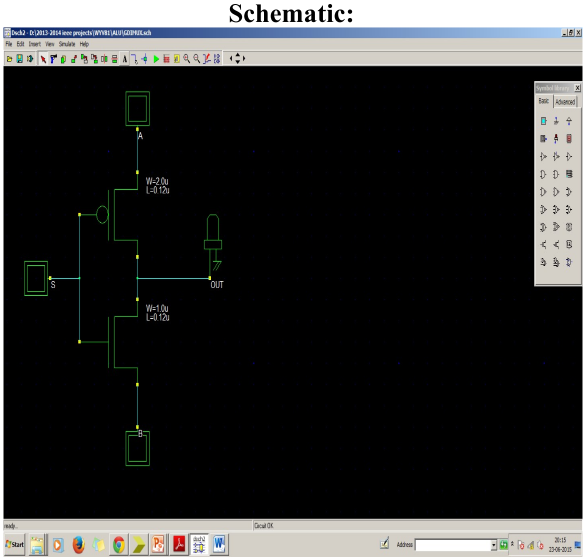
256 ns to precisely cover all changes once. Fig. 8 delineates the information/yield wave-types of our proposed 2– 4 decoders for each of the 16 input advances, showing their full swinging capacity.

B. Execution Metrics Examined

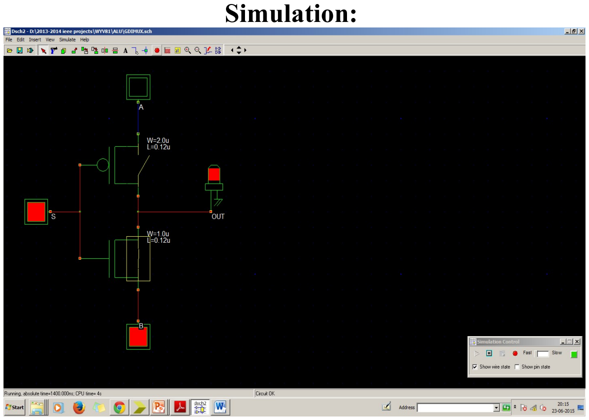
The measurements considered for the correlation are: normal power dispersal, most pessimistic scenario deferral and power-postpone item (PDP). With persistent sub-micron scaling and low voltage task, spillage control has turned out to be progressively critical as it commands the dynamic one [12]. In our examination, both spillage and dynamic streams are viewed as and the aggregate power dispersal is separated from flavor recreation, estimated in nanowatts (nW). Concerning, we take note of the most elevated esteem that happens among all I/O advances, estimated in picoseconds (ps). At long last, PDP is assessed as normal power*max delay and estimated in electron volts (eV).

Results and investigation: GDI_MUX:

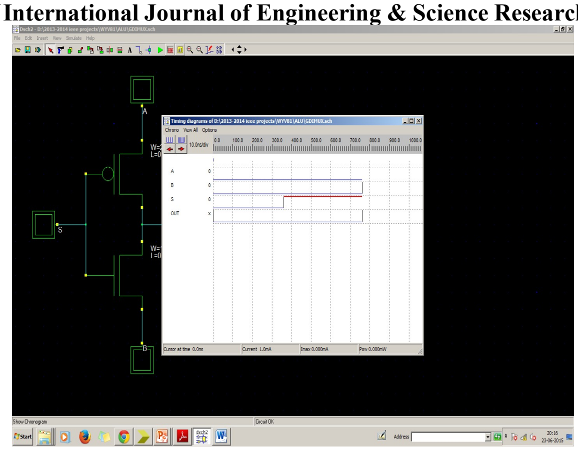
Schematic:



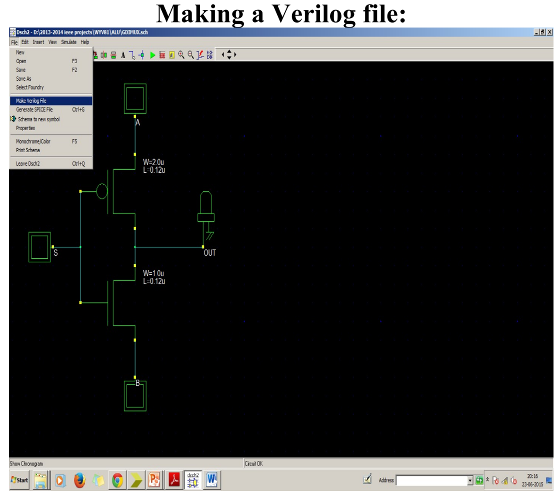
Simulation:



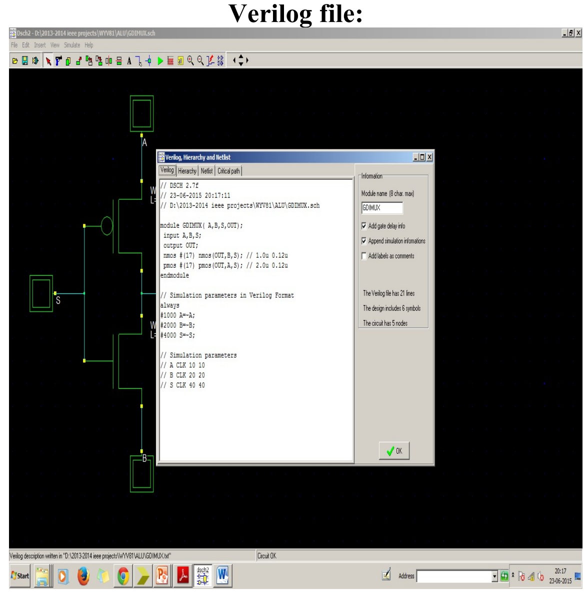
Characteristics:



Making a Verilog file:



Verilog file:



Layout of GDI MUX:

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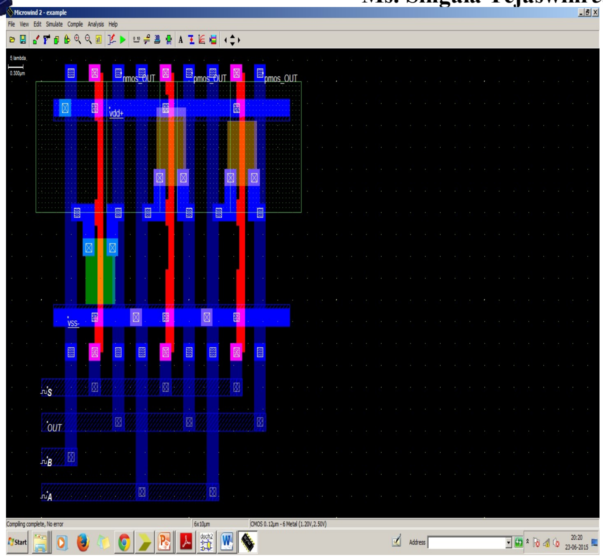

Simulate:

Result & Discussion

The recreation results in regards to power, PDP and postponement are appeared in Tables III– V, separately. Each of the proposed de-signs will be contrasted with its traditional partner. Specif-ically, 2– 4LP and 2– 4HP are contrasted with 20T, 2– 4LPI and 2– 4HPI are contrasted with upsetting 20T, 4–16LP and 4– 16HP are contrasted with 104T lastly, 4– 16LPI and 4– 16HPI are contrasted with rearranging 104T.

As indicated by the got results, 2– 4LP presents 9.3% less power dissemination than CMOS 20T, while presenting an expense of 26.7% higher postponement and 15.7% higher PDP. Then again, 2– 4HP beats CMOS 20T in all perspectives, diminishing force, deferral, and PDP by 8.2%, 4.3%, and 15.7%, separately. Both of our rearranging plans, 2– 4LPI and 2– 4HPI, beat CMOS 20T modifying in all viewpoints also. In particular, 2– 4LPI diminishes power, postponement, and PDP by 13.3%, 11%, and 25%,

Table 3
Power Dissipation Results (In Nanowatts)

2-4 DEC.	500MHZ			1GHZ			2GHZ			4-16 DEC.	500MHZ			1GHZ			2GHZ		
	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V		0.8V	1.0V	1.2V	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V
CMOS	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	CMOS	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2-4LP	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	4-16LP	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2-4HP	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	4-16HP	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
CMOS INV.	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	CMOS INV.	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2-4LPI	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	4-16LPI	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2-4HPI	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	4-16HPI	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

Table 4
Pdp Results (In Electronvolts)

2-4 DEC.	500 MHZ			1GHZ			2GHZ			4-16 DEC.	500 MHZ			1GHZ			2GHZ		
	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V		0.8V	1.0V	1.2V	0.8V	1.0V	1.2V	0.8V	1.0V	1.2V
CMOS	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	CMOS	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2-4LP	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	4-16LP	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2-4HP	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	4-16HP	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
CMOS INV	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	CMOS INV.	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2-4LPI	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	4-16LPI	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
2-4HPI	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	4-16HPI	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

Table 5
Propagation Delay Results (In Picoseconds)

	0.8V	1.0V	1.2V	4-16 DEC.	0.8V	1.0V	1.2V
CMOS	105	49	33	CMOS	214	97	66
2-4LP	132	62	43	4-16LP	203	93	64
2-4HP	99	47	33	4-16HP	195	88	59
CMOS INV	100	48	34	CMOS INV.	252	108	71
2-4LPI	89	43	30	4-16LPI	270	119	79
2-4HPI	87	42	29	4-16HPI	243	107	71

Conclusion

This research introduces a novel hybrid logic design strategy for line decoders that effectively integrates **Transmission Gate Logic (TGL)**, **Dual-Value Logic (DVL)**, and **static CMOS logic**. Leveraging this approach, four new 2-to-4 line decoder topologies — **2-4LP**, **2-4LPI**, **2-4HP**, and **2-4HPI** — have been developed. These designs demonstrate notable improvements over conventional CMOS implementations by achieving lower transistor counts and enhanced delay characteristics.

Building upon these optimized 2-to-4 pre-decoders, four new 4-to-16 line decoder architectures — **4-16LP**, **4-16LPI**, **4-16HP**, and **4-16HPI** — have also been proposed. These designs utilize the hybrid 2-to-4 pre-decoding stage followed by robust static CMOS post-decoding logic to ensure strong output drive capability and reliable performance.

Extensive simulations conducted at the **32 nm technology node** confirm that the proposed hybrid decoders consistently outperform traditional CMOS designs across critical metrics, including power consumption, propagation delay, and Power-Delay Product (PDP). Among the developed topologies:

The **2-4LP** and **4-16LPI** variants are particularly well-suited for area- and power-constrained applications.

The **2-4LPI**, **2-4HP**, and **2-4HPI** configurations deliver strong overall performance, making them ideal for a broad range of use cases that demand balanced power-speed trade-offs.

Thanks to their low power dissipation and optimized transistor usage, these decoder designs are highly suitable for integration into large-scale digital systems, including multiplexers, hierarchical memory address decoders, and other complex combinational logic blocks with diverse performance requirements.

Furthermore, the proposed architectures are compatible with both bulk CMOS and Silicon-on-Insulator (SOI) process technologies. Their modular and efficient structure also makes them excellent candidates for inclusion in standard cell libraries and seamless integration at the Register-Transfer Level (RTL) in modern VLSI design flows.

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