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Full Length Article

Performance-Oriented CMOS Multiplexer Layout Optimization Process

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Abstract
*Multiplexer circuits are fundamental building blocks in modern digital systems and play a vital role across various domains of engineering, particularly in digital design and communication systems. In the field of **Very Large-**Scale Integration (VLSI), there is a continuous drive to reduce design complexity, development time, and overall resource utilization while maintaining high performance. This project focuses on the design and implementation of a 2-to-1 multiplexer using CMOS (Complementary Metal-Oxide-Semiconductor) logic, with the objective of developing a more efficient, compact, and optimized circuit architecture. The study explores multiple design approaches to achieve significant improvements in key performance parameters, including power consumption, circuit complexity, propagation delay, and silicon area. A detailed comparative analysis is carried out using 35 nm technology, which allows for a realistic evaluation of how nanoscale fabrication processes influence the behavior and efficiency of the multiplexer design.*
Special emphasis is placed on area optimization, as reducing the physical footprint of digital circuits is critical for improving integration density and lowering manufacturing costs in VLSI systems. By critically examining and refining different logic design methodologies, this work aims to contribute a streamlined and practical solution for multiplexer implementation that balances performance with resource efficiency. The proposed design not only demonstrates improved characteristics compared to conventional approaches but also highlights the importance of careful architectural choices in nanoscale CMOS technology for next-generation digital systems.

Key Words: *MUX, Pseudo NMOS logic Low Power, Static CMOS logic, Low Power.*

Introduction:
The VLSI (Very large scale integration) is an important tool to integrate the number of components on a single chip. The choice of design style of VLSI product depends on the performance requirement, the technology being used, the lifetime and cost of the project. The important factors are area reduction, minimum power consumption and high speed. Now days, the demand for these factors are increasing. There are many design techniques are developed to enhance the performance of logic circuits. The operation in high temperature environment results in silicon failure and the circuit will be damaged. So, the requirement for low power consumption is increasing with the growth in devices like Mobile phones, medical instruments and Cs. Another factor is power consumption, which should be minimized because it results in low electricity consumption and less amount of heat is produced. [3] Multiplexer is major component in telecom industry and it‟s a key component of any arithmetic circuit. These are building blocks for data switching structure with resource sharing. In a communication system, the transmission takes place between transmitter and receiver by using a multiplexer at the transmitter side to transmit the data from many users on a single channel with the help of selection (control) lines.[4]
The field of field-programmable gate arrays (FPGAs) grew out of the PROM and PLD industries (PLDs). Any programmable logic device (PLD) or programmable read-only memory (PROM) could be modified in groups at a manufacturing facility or in the field. The Naval Surface Warfare Department supported Steve Casselman's early proposal in the late 1980s to create a personal computer capable of running 600,000 reprogrammable entries. In 1992, a patent was issued for the structure thanks to Casselman's efforts. The licenses granted for business central ideas and advancements for a programmable method of reasoning bundles, entryways, and justification squares.

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1. Multiplexer:

Multiplexer is a combinational logic circuit, in which the output is generated from one of the various inputs. Multiplexer is abbreviated as MUX. A practical application in which many users are requested to use a single channel to send their data, in that case multiplexer has ability to multiplex all signals and transmit on a single channel. So, it also called a data selector, to select the number of inputs one by one to provide a single output. The selection lines control routing of data input to the output.

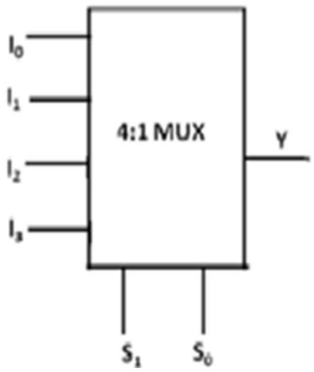

Fig1- 4:1 MUX

The 4:1 MUX consists of 4 external inputs with two selected lines to provide single output. An intelligent multiplexer is referred to concentrator in the telecom world. Multiplexers are used for switching application, A/D convertor, telephone network and Digital semiconductors. [5] Multiplexers can be used as programmable logic devices. The circuit is combining two or more digital signals to give a single line. [6]

Table 1- 4:1 MUX truth table

Selection lines		Output
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

The above table (1) shows the truth table for 4:1 MUX which consists of 4 combinations of input.

By using, $(4 = 2^2)$ 2 selection lines are required to design 4:1 Multiplexer. Boolean expression for 4:1 MUX is written as:-

$$Y= I_0S_1\ S_0 + I_1\ S_1\ S_0 + I_2\ S_1S_0 + I_3\ S_1S_0$$

are the inputs applied to multiplexer, S0 and S1 are selection lines, Y is the output of the multiplexer

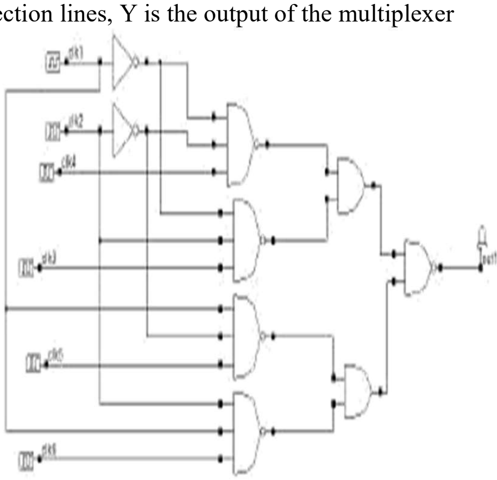

Fig2- 4:1 MUX Schematic

In above Schematic, clock are used to provide input and LEDs (light emitting diode) to test the output. For hardware implementation, it requires four 3-input NAND gate and a 4-input NAND gate with two inverters to generate the complement of S1 and S0.

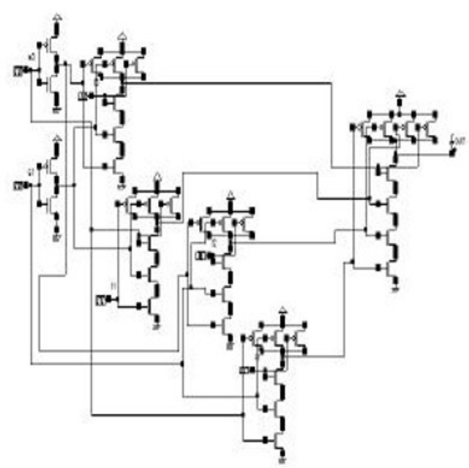

Fig.3- 4:1 MUX using CMOS

The circuit can also build with CMOS technology. It has been designed with implementing PMOS & NMOS transistors. In CMOS circuit, there is low power dissipation during switching operation of the device. The PMOS & NMOS transistors form the pull up and pull down network respectively. It is made by combining of NMOS and PMOS transistors with four external inputs (I0, I1, I2, I3) and normal & complemented inputs of S1 and S0 as selection lines to provide single output.

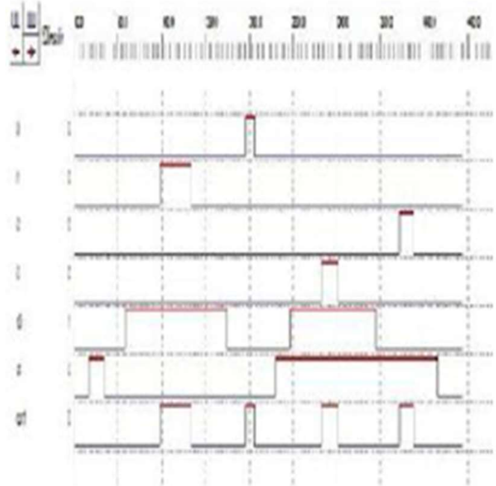

Fig.4- 4:1 MUX output

The above waveform is of 4:1 multiplexer, generated in DSCH in which s1 & s0 are control lines, (i0, i1, i2, i3) are input and out1 is output.

2. Layout Design:

DSCH3 & Micro wind are the CAD tools have been used to implement 4:1 MUX using NAND gate. Before the layout of 4:1 MUX, the schematic of circuit must be validate. The solution of this problem is taken by Dsch & micro wind. Dsch is a simulator for the simulation of logic design and to understand the proper function of the circuit. Then, the layout is created in micro wind. [8]

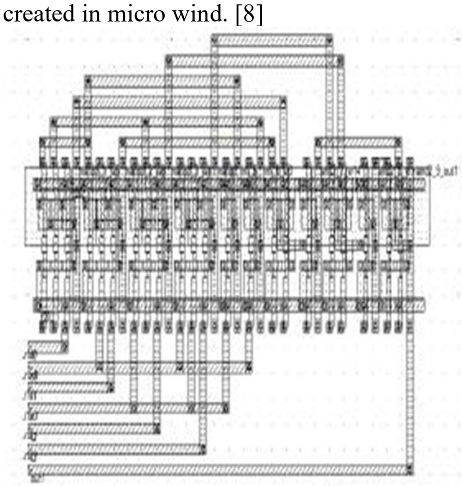

Fig.5- Auto generated layout of 4:1 MUX

This layout occupied the area of 432.2µm2 with power consumption by 25.645µw. The created layout can also be possible by semicustom design level.

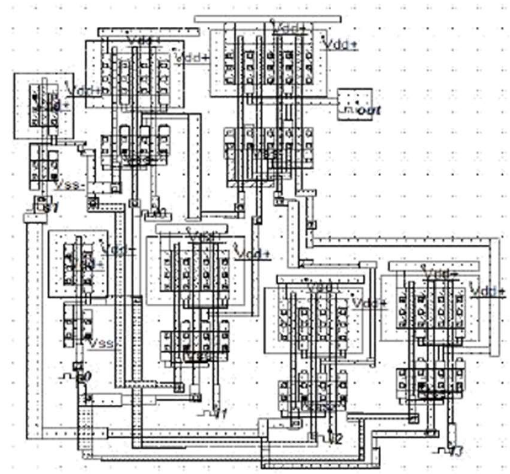

Fig.6- Semicustom layout of 4:1 MUX

The semicustom layout of 4:1 MUX is shown in the figure can be designed by different technologies 90nm. This layout occupies the area of 107.4µm2 with power consumption of 23.937µw in 90nm technology . Simulations have been done with micro wind 3.1 tool and it is performed on the layout of Semicustom design level. The logic „0" and logic „1" corresponds to low and high level respectively. Clocks are applied as inputs and selection lines.

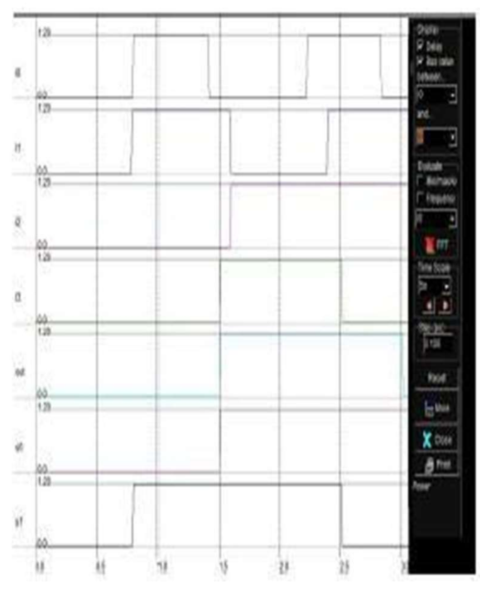

Fig.7- Waveform of 4:1 MUX for semicustom design

The 4:1 multiplexers have been designed by auto Generated and semicustom design tools. These are simulated and compared in terms of its power consumption and area at 90nm.

Table2- Comparison in terms of power and area

Technologies	Power	Area
Autogeneration (90nm)	25.645μw	$432.2\mu m^2$
Semicustom (90nm)	23.937μw	$107.4\mu m^2$

It has been observed that 4:1 multiplexer using Semicustom design level has low power consumption as compared to Auto generated design.

4. Proposed Multiplexer Using Cmos

There are two types of MOS, i.e. the NMOS and the PMOS. Where NMOS transistor can gives the "LOW" signal completely, but it has poor performance at "HIGH" signal. Same as in PMOS transistor which gives the "LOW" signal completely but poor performance at "HIGH" signal. CMOS transistor is the combination of NMOS and PMOS transistor which gives full output voltage swing. Power consumption is very less in CMOS circuits compared to the NMOS design and bipolar transistors. There are different design methodologies of designing of integrated circuit such as full custom design, semi custom design and standard cell based design.

In standard cell design, a design is captured using the standard cells available in a library via schematic or HDL [2]. In the full custom design the function and layout of practically every transistor is optimized. This paper is based on the area efficient design 2 to 1 multiplexer using Micro wind tool. The schematic diagram of 2:1 MUX is as shown in fig.3.1.This circuit is designed with the help of universal NAND gates where 7 PMOS and 7 NMOS are used. The total numbers of 14 transistors are used in the CMOS design. P Switch is connected to the Vdd to the output and N switch is connected to the output to Vss [2]. In this CMOS design NMOS works as pull down network and PMOS works as pull up network.

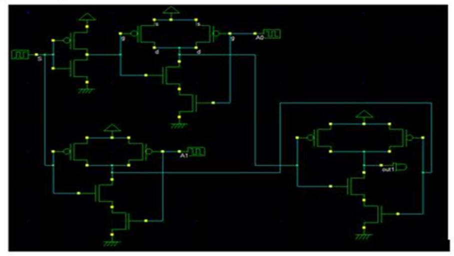

Fig.3.1 Schematic of 2 To 1 Multiplexer Using NAND Gates

Fig.3.2 shows the standard cell multiplexer layout design. Standard cell multiplexer design is complex and consumes more area.

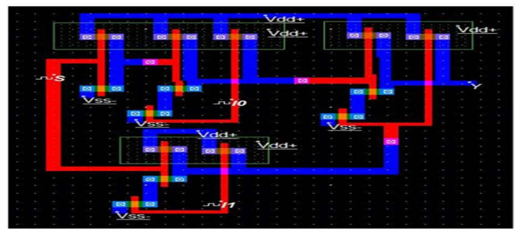

Fig.3.3 Semi Custom Design Of 2 To 1 Multiplexer

5. Comparative Analysis

The main parameters of consideration are area, complexity and power of the 2 to 1 multiplexer in this paper. Table 4.1 shows the area and power consumption of 2 to 1 multiplexer circuit.

Table 4.1 Area and Power consideration

Multiplexer Layout	Technology Used	AREA Used	POWER Consumption
Standard Cell Based Design	35nm	696.3μm2	46.800μW
Semi Custom Design	35nm	593.9μm2	0.336mW
Full Custom Design	35nm	359.1μm2	0.142mW

Here 35nm technology is used in the designing of standard cell based layout, semi custom based layout and full custom layout of 2 to 1 multiplexer with the help of Microwind tool. Transistor width (w) = 0.200 micrometer and length L=0.100 micrometer has been used in the design.

Conclusion:

study successfully explored and compared three different design methodologies for implementing a 2-to-1 multiplexer: conventional cell-based, semi-custom, and fully custom layouts. Each approach offers distinct advantages depending on the design priorities.

The comprehensive evaluation, based on key performance metrics such as circuit complexity, silicon area occupation, and power consumption, clearly indicates that semi-custom and fully custom designs are significantly more efficient than the traditional cell-based approach. Notably, the fully custom layout demonstrated superior power efficiency, achieving approximately 35.67% lower power consumption compared to the semi-custom design.

These findings emphasize the critical importance of selecting an appropriate design methodology in VLSI circuits. By moving beyond standard cell-based implementations toward semi-custom and fully custom strategies, designers can achieve substantial improvements in power efficiency and area utilization without compromising functionality. The results of this research provide valuable insights for low-power digital circuit design and highlight the potential of optimized layout techniques in addressing the growing demand for energy-efficient VLSI systems

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