

Performance Evaluation Of Proposed Compressor Architectures In Multiplier Designs

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Abstract

This research introduces advanced higher-order compressor architectures specifically optimized for high-speed and energy-efficient multiplication operations in VLSI systems. The proposed designs deliver two primary advantages: significantly reduced computational latency and improved spatial (area) efficiency within the multiplier structure. While lower-order compressors generally achieve a marginally better Energy-Delay Product (EDP), their inherent limitations in delay and area make them less suitable for high-performance applications. The trade-offs between EDP, speed, and silicon area must therefore be carefully evaluated based on the specific requirements of the target application. To thoroughly assess the effectiveness of the proposed 8-4 and 9-4 compressors, the study implemented and analyzed multipliers of varying sizes: 8×8 , 16×16 , and 24×24 . These were systematically compared against conventional multiplier architectures that rely on traditional lower-order compressor structures. Simulation results clearly demonstrate that the newly developed compressors deliver superior performance in scenarios demanding fast multiplication. They achieve noticeable improvements in overall speed and area utilization, making them highly effective for modern high-performance digital systems. The proposed higher-order compressor designs successfully address many of the shortcomings associated with conventional approaches. By offering a better balance between speed, area, and power efficiency, they represent a meaningful advancement in multiplier optimization. These architectures are particularly well-suited for integration into high-speed processors, digital signal processors (DSPs), and other performance-critical VLSI applications where both latency and area constraints are paramount. The findings from this research contribute valuable insights for future development of low-power, high-speed arithmetic circuits and reinforce the importance of innovative compressor designs in advancing VLSI technology.

Keywords— VLSI design, higher-order compressors, 8–4 compressor, 9–4 compressor, high-speed multiplier, energy-delay product (EDP), area optimization, low-power design, digital signal processing (DSP), arithmetic circuits.

Introduction

VLSI remains for "Critical Scale Integration". This is the field which joins pressing continuously technique for thinking contraptions into increasingly little and littler areas. VLSI, circuits that would have consumed boardfuls of room would now have the ability to be put into a little space couple of millimeters over! This has opened up an important chance to do things that were implausible heretofore. VLSI circuits are all over the place .your PC, your auto, your fresh out of the plastic new top level automated camera, the mobile phones, and what have you. This consolidates a ton of bent on different fronts inside a practically identical field, which we will take a gander at in later bits. VLSI has been around for quite a while, yet as a reaction of advances in the space of PCs, there has been an eager improvement of contraptions that can be utilized to format VLSI

circuits. Close by, consenting to Moore's law, the point of confinement of an IC has expanded exponentially reliably, to the degree estimation control, a usage of accessible territory, yield. Mix enables us to deliver frameworks with different more transistors, engaging through and through furthermore enlisting capacity to be related with managing an issue. Made circuits are moreover essentially less mentioning to plan and make and are more dependable than discrete structures; that makes it conceivable to make remarkable reason frameworks that are more convincing than completely accommodating PCs for the action that ought to be done.

Literature Review

Ultra Low-Voltage Low-Power CMOS 4-2 and 5-2 Compressors for Fast Arithmetic Circuits [2004] In this paper the maker presents distinctive models

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and blueprints of low-control 4-2 and 5-2 blowers prepared for working at ultra low supply voltages. Each designing has unmistakable courses of action fuses different novel 4-2 and 5-2 blower plans. They are prototyped and imitated to survey their execution in speed, control dispersal and power-delay thing. The proposed new circuit for the XOR– XNOR module delineated in this paper takes out the weak method of reasoning on the inside center points of pass transistors with a few info NMOS– PMOS transistors. Driving limit has been considered in the blueprint and furthermore in the reenactment setup with the objective that these 4-2 and 5-2 blower cells can work constantly in any tree composed parallel multiplier at low supply voltages. In this paper the maker construe that a phenomenal disappointment control circuit with extraordinary drivability is proposed for the complex XOR method of reasoning module which is used to co-produce the XNOR-XOR yields. Novel 5-2 blower structure of deferral is also proposed. Another arrangement of the pass on generator cell has been delivered in view of this novel designing.

Novel and Efficient 4:2 and 5:2 Compressors with Minimum number of Transistors Designed for Low-Power Operations [2006]

This paper proposes beneficial and perfect 4:2 and 5:2 blowers. The blowers are significantly redesigned the extent that transistor check. These plans have the standard ideal position that despite reduced change development, they have no quick relationship with the power-supply and is totally dictated by the data signals, inciting a noticeable diminishing in obstruct usage. The proposed 4-2 and 5-2 blower blueprints have been executed with an outright least of 20 and 30 transistors independently. The speed, an area and power usage of the multipliers will be in guide degree to the efficiency of the blowers. This paper gives novel plans of 4:2 and 5:2 blowers with least number of transistors. The proposed layouts are outstandingly viable to the extent little domain low power and high throughput. In this paper, the maker at first depicted about the present structure of 4:2 and 5:2 blowers. In the proposed blower plan, the XOR portal and MUX plots are appropriately superseded with least transistor utilization to diagram the circuit to such a degree, that it has no quick supply from VDD. It will in general be interpreted that the proposed 4:2 blower design is an upgraded structure as the makers have streamlined the entire diagram starting from the central cell level.

A Novel High-Speed and Energy Efficient 10-Transistor Full Adder Design [2007]

In this paper, the maker proposed a full snake design using only ten transistors for each piece. The proposed design features cut down working

voltage, higher figuring speed and lower essentialness action when differentiated and existing techniques. The arrangement uses inverter bolstered XOR/XNOR diagrams to take out the edge voltage mishap issue. This issue shields the full snake from working in low supply voltage. The proposed arrangement embeds the buffering circuit in the full snake plan and the transistor count is restricted. The upgraded buffering works under lower supply voltage differentiated and existing works. It also overhauls the speed execution of the fell action basically while keeping up the execution edge in essentialness use. Both dc and displays of the proposed diagram against various full snake plans are surveyed by methods for expansive HSPICE propagations.

Compressors

Augmentation is a basic task in the majority of the flag handling calculations. Multipliers have substantial zone, long inertness and devour significant power and the plan of good multipliers is dependably a test for VLSI framework planners. The target of a decent multiplier is to give a physically reduced, great speed and ought to expend low power. Increase comprises of three stages (I) Partial item age (ii) Partial item decrease (iii) Final item calculation. Decrease of halfway item stage will influence the multiplier execution as far as speed and power scattering in the VLSI circuits. Halfway item decrease has high latencies because of the long vertical way. Ordinarily adders are utilized to lessen the vertical basic way. In any case, adders will make issues like glitches, uneven flag change; and it will take more number of stages to diminish the incomplete item decrease. To stay away from those issues, blowers should be executed in the multiplier plan. (Oklobdzija ET AL., 1996; Dandapat ET AL., 2007). The upside of utilizing blowers is to give customary structure in fractional item decrease organize.

The lower arrange blowers, for example, 3 - 2, 4 - 2, 5 - 2 were considered by numerous scientists (Dandapat ET AL.,

2010) and (Veeramachaneni ET AL., 2007). In rapid multiplier, 4-2 blowers have been broadly used to bring down the dormancy of the halfway item decrease stages. The majority of the business outlines in the different processors in the market utilize 4 to 2 blower. Indeed, even the quantity of incomplete item decrease stages can't be diminished as much utilizing the lower arrange blowers. Thus the postponement of multipliers additionally was not diminished to such an extent. The higher request blowers (5-3, 6-3 and 7-3) were utilized to enhance the execution of multipliers prior (Dandapat ET AL., 2010; Dadda, 1976). They have combined double counter property into the

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high request blowers which have additionally decreased the halfway item stages and power utilization. In this examination, we have utilized 7 3 blower which is outlined by four full adders (Dadda, 1976) to enhance the execution of multiplier. In this investigation, we have proposed 8-4 and 9-4 blowers which have additionally diminished the quantity of incomplete item phases of multipliers when contrasted with existing blowers. Also, the proposed blowers utilize less number of doors, so generally plan territory diminishes. This procedure offers less deferral, however Energy Delay Product (EDP) is somewhat higher than bring down request blower.

The 4-2 blower has five information sources and creates two yields and one do. This blower utilizes two phases of full adders associated in arrangement. This straight forward usage has four XOR door delays. (Oklobdzija ET AL., 1996). Different methodologies have been proposed to enhance their speed. As, 4-2 blowers were executed with 3 XOR delays (Hsiao ET AL., 1998; Gu and Chang, 2003; Chang ET AL., 2004; Ma and Li, 2008).

Confinements of Lower Order Compressor Design

It is required to make a note of the impediments of existing lower arrange blowers, for example,

- They require more adders to figure the correct paired weighted yield results
- It is required to include half viper with a 4-2 blower and a full snake with a 5-2 blower to get appropriate parallel weighted outcomes
- Uneven flag engendering into the adders prompts some undesirable changes which increment dynamic power utilization
- The third phase of full snake needs some additional time (say Δ) to register the last aggregate and out c. Time Δ will be more for 6-2 and 7-2 blowers

Proposed Compressor Design

The proposed higher request blowers, 8-4 and 9-4 give preferable execution over the lower arrange blowers as far as speed and zone. A portion of the restrictions said above have been limited in 7-3 blower (Dadda, 1976). In any case, the deferral can be additionally diminished by utilizing 8-4 and 9-4 blowers. We have created 8-4 and 9-4 blowers for multipliers. A right mix of snake has been produced a proficient 8-4 and 9-4 blowers.

3.3. Structure of 8-4 and 9-4 Compressors

Utilizing full and half viper Fig. 1 demonstrates that 8-4 blower has 8 inputs (I0-I7) and four yields (X1-X4). This blower utilizes counter property so that, yield of blower gives number of 1's at input. For instance, if all info bits are 1, at that point yield of the blower is "1000". In this plan, blower takes four phases of adders to pack the info bits into four

yield bits. In first stage, two full adders and one half adders are utilized in parallel. Two full adders are utilized in second stage. All "Sum" yields from the main stage are sustained with one full viper and all "Carry" yields are bolstered to another snake. One half snake is utilized in third and fourth stage to create the outcome. Absolutely, we have utilized four full adders and three half adders.

For instance, 4-2 blower takes four phases and six full adders to pack 8 bits into 4 bits. Proposed blower has more number of half adders. Half snake frequently utilizes less number of doors and possesses less zone than full viper.

The basic way deferral of the proposed execution is 6 XOR door delay. The conditions administering the yields in the proposed 8-4 design are appeared underneath Equation (1 to 4):

yields in the proposed 8-4 design are appeared underneath Equation (1 to 4):

$$\mathbf{x}_1 \square \mathbf{a} \oplus \mathbf{c} \oplus \mathbf{e} \quad (1)$$

$$\begin{array}{c} \square \square \square \square \text{ ac} \\ \text{x2ac} \square \square \square \square \mid \square \square \square \square \mid \square \square \square \square \oplus \square \square \square \square \oplus \square \square \square \square \oplus \square \square \square \square \end{array} \quad (2)$$

$$\begin{array}{cccc|cccc|cccc|cccc|} x_3 & \square & \square & \square & \square & ae & \square & ce & \square & \square & \square & b & \oplus & d & \oplus & f & \square & bf & \square & df \\ ac & \square & & & & \square & & \square \oplus \square & \square & bd & \square & & & & & & \square & & \square \square \end{array} \quad (3)$$

$$\begin{array}{ccccccccc|ccccccccc} \square & \square & \square\square & \square & ae & \square & ce & \square & \square & \square & \square & b \oplus d \oplus f & \square & bf & \square & df \\ x4ac & \square & & & \square & & \square & \square & \square & \square & bd & \square & \square & \square & \square & \end{array} \quad (4)$$

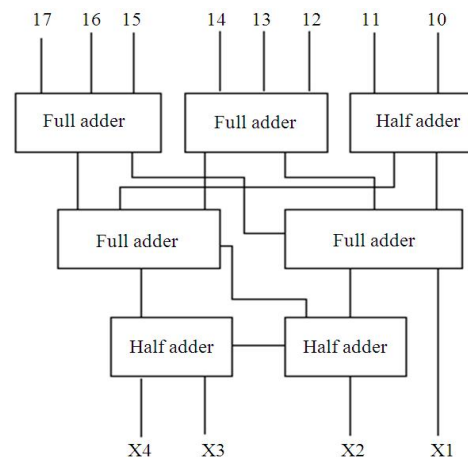


Fig. 1 Compressor design

The essential path deferral of the proposed 9-4 blower is 6 XOR entryway delay and the amount of lessening stages is

A. Main focal points of the proposed blowers than low solicitation blowers are, (1) Uniform XOR gateway concede paying little regard to the information bits (2) Number of

reduction arrange is less (3) Less number of entryways.

Structure of 8-4 and 9-4 Compressors Using Multiplexer

This structure is recognized in light of the help of multiplexer keeping the ultimate objective to hint at progress result similarly as power dispersal and imperativeness delay thing. Figure 3, 4 and Table 1 exhibits the utilization of 8-4 and 9-4 blowers.

In a multiplexer, using the assurance lines only the bit of the structure is dynamic, letting the rest well enough alone for rigging mode. Thusly saving critical proportion of power and appropriately diminishing the imperativeness concede thing by various folds.

Multiplexer Architecture

We have laid out three one of a kind (8×8 , 16×16 and 24×24) multipliers using Wallace tree building (Law ET AL., 1999). These multipliers uses higher solicitation blowers. Figure 5 demonstrates plan of a 16×16 multiplier. Differing sorts of blowers are used to enroll the fragmentary thing. Partial things are incorporated five stages. Proper arrangements of blowers/adders have been used remembering the true objective to decrease the vertical essential way. Allow us to consider fragment number fifteen of Fig. 5, which has fifteen bit things. We can use one 7-3 and 6-3 blowers and half snake to that portion. This mix produces eight yields. As opposed to that, one 8-4 and 7-3 blowers could be a predominant decision. This mix makes only seven yields. By picking suitable blend of blowers/adders, we can restrain the fundamental way.

Vertical box demonstrates the blowers/snake. In case any of the portions isn't campaigned in the cases, those things can be passed to the accompanying stage. In case the case is even in bearing, it shows that the parallel adders have been used. We have used swell pass on adders in parallel snake. All of the three multipliers are arranged capably. We have made the multiplier which has less number of adders/blowers. By and by let us consider fragment 31 which has two vertical touches and area 32 which has one spot. Instead of using one half adders in section 31, we explicitly incited those two spots into the accompanying stages. This restricts the amount of adders in the multiplier.

Multiplexer Performance and Comparison

We have used 3-2 (Hsiao ET AL., 1998) and 4-2 blowers of (Chang ET AL., 2004; Ng and Lau,

1999; Prasad and Parhi, 2001; Baran ET AL., 2010; Ma and Li, 2008) in our 8 bit, 16 bit and 24 bit multipliers and found that our proposed higher solicitation blowers give higher speed and lesser district Table 2. Figure 6-8 independently exhibits the speed, locale and power examination of a multiplier using both low and high solicitation blowers. Speed of the higher solicitation blower multiplier increases when duplication bit increases. For 8 bit expansion the speed change is 4% than low solicitation blower diagram. Basically, speed change of higher solicitation blower for 16 bit is 9.04 and 9.3% for 24 bit multiplier. High solicitation blowers have less passage count and it includes less region than standard blowers. High solicitation blower eats up more power than low solicitation blower. For 8bit, 16 bit and 24 bit multiplier the power usage is extended by 10, 22.6 and 26.7% independently.

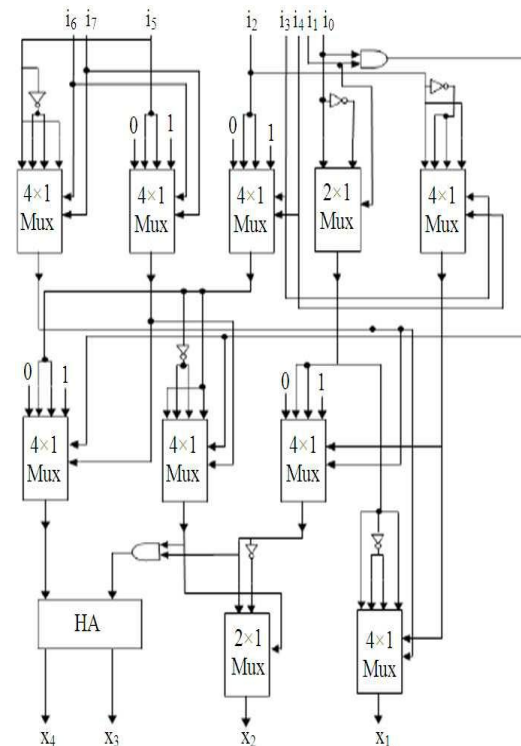


Fig.2. Implementation of 8-4 compressor using multiplexer

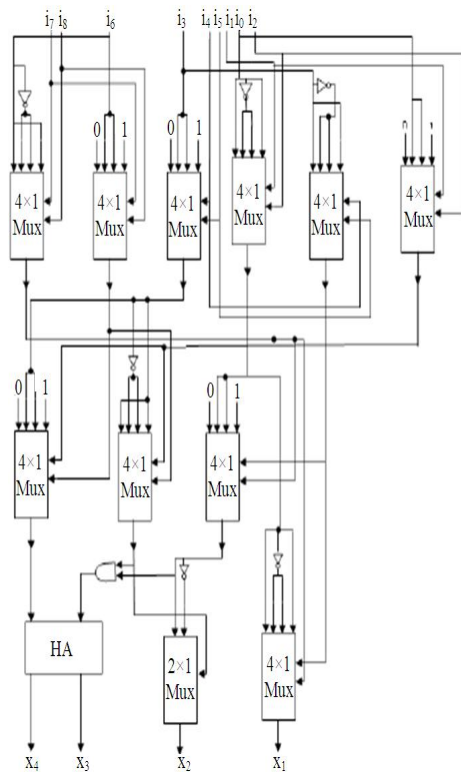


Fig.3; Implementation of 9- 4 compressor using multiplexer

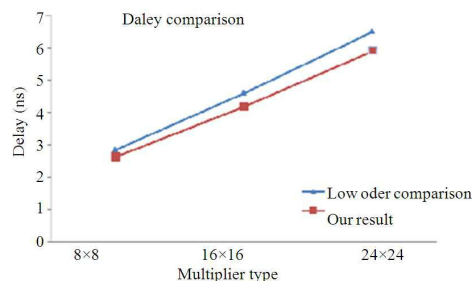


Fig. 4; Speed comparison of different multiplier

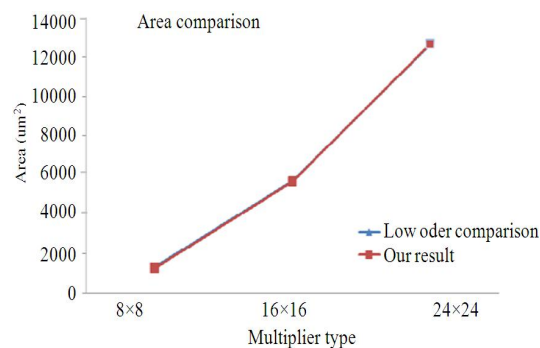


Fig.5; Area comparison of different multiplier

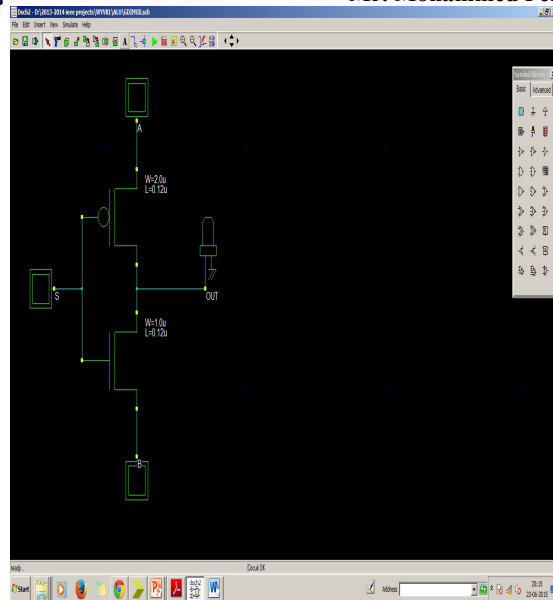
In the diversion results show that the 8-4 and 9-4 blowers worked with the novel XOR cell can work down to 0.6 V, and features quick and low-control characteristics. The 5-2 blower proposed by the maker beats the different models. The maker traces that a library of incredible power capability 4-2 and 5-2 blower cells in light of CMOS process advancement has been delivered for realizing fast and low-control multipliers operable at ultra low supply voltages. In the diversion is done in Tanner season and the development being used is 0.35-um CMOS propelled advancement with a 3.3-V supply voltage. The inciting delay is assessed when the changing data accomplishes half of the advancement to when the yield accomplishes its half. Finally the maker construed that the proposed layouts have the good position that despite diminished change development, they have no quick relationship with the power-supply and are totally dictated by the data signals, provoking a conspicuous reduction in hamper use.

In the amusement results rely upon TSMC 2P4M 0.35-m process models, show that the proposed arrangement has the least working Vdd and most astonishing working repeat among all layouts using 10T. It similarly shows the power use is low per development among these frameworks. What's more, besides, the execution edge of the proposed blueprint in both speed and imperativeness usage ends up being significantly more vital as the word length of the snake increases. The CLRCL design requires the most negligible power supply among every one of the 10T frameworks. The CLRCL arrangement has the fit for the most critical working repeat. In all of the multiplications have been done using Cadence Tools with 0.18-um development. The calculation of force (tallying glitch power) and deferral are finished using the Virtual Analog Simulation instrument adequately organized into Cadence Tools. The reenactments are performed under various voltages reaching out from 0.9V to 3.3V. The proposed models perform better than the present ones in every viewpoint i.e., region, power, deferral and power-delay thing over the complete voltage run reenacted.

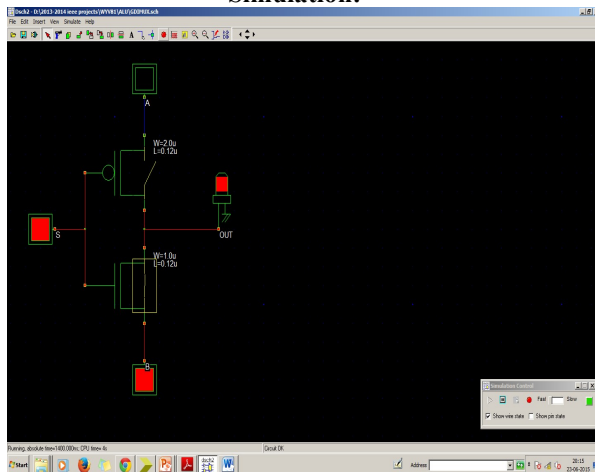
Results and analysis:

GDI_MUX:

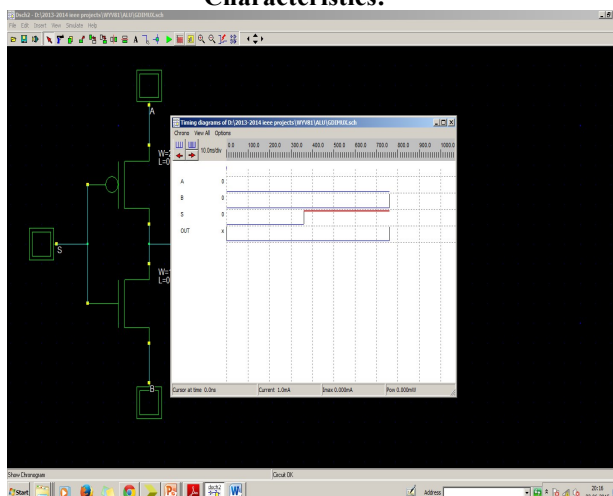
Schematic:



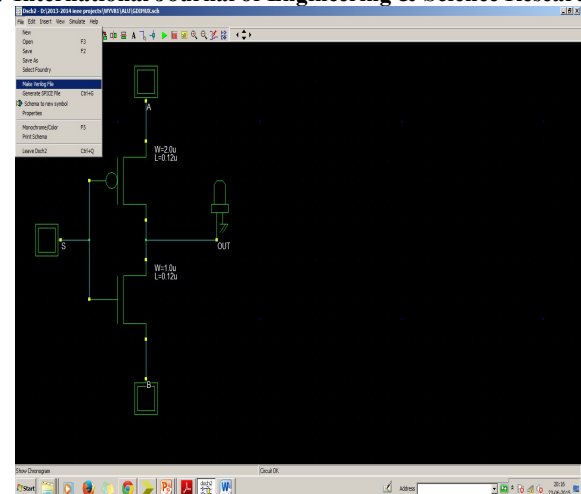
Simulation:



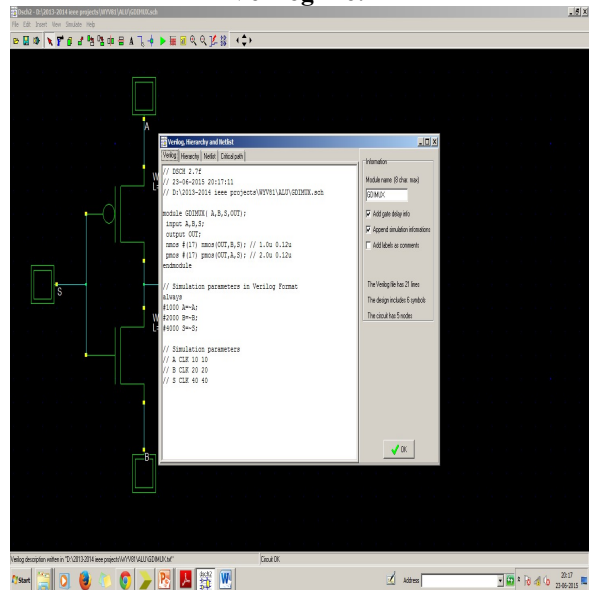
Characteristics:



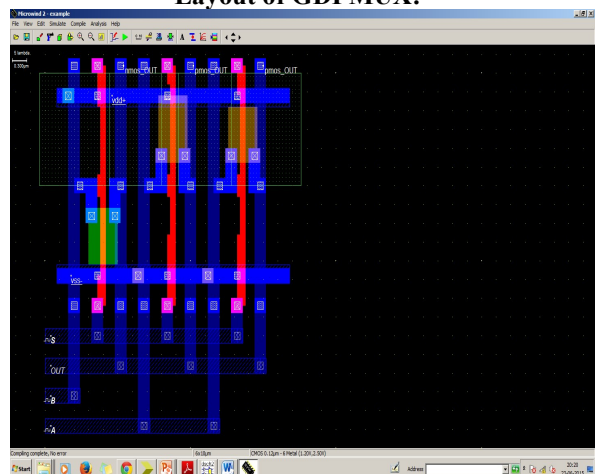
Making a Verilog file:



Verilog file:



Layout of GDI MUX:



Simulate:

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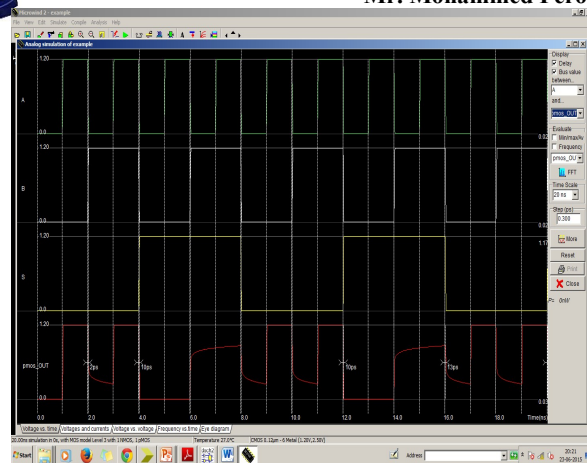
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Conclusion

In conventional multiplier designs, lower-order compressors are commonly employed during the partial product reduction phase. While effective to a certain extent, this approach often results in non-uniform signal propagation throughout the multiplier structure. Such irregularity can lead to increased switching activity, timing imbalances, and higher dynamic power consumption.

To overcome these limitations, **higher-order compressors** have been developed as a more efficient solution. By reducing the total number of reduction stages and shortening the critical vertical paths, these advanced compressors significantly improve overall multiplier performance. The proposed 8-4 and 9-4 compressor architectures further enhance this approach by utilizing a reduced number of logic gates. This optimization results in notable improvements in both processing speed and silicon area utilization compared to traditional lower-order designs.

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