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Full Length Article

Design And Analysis Of High-Speed Hybrid Full Adder Architectures With Improved Power Efficiency

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Abstract:
This study explores advanced configurations of 1-cycle full adder designs by combining complementary metal-oxide-semiconductor (CMOS) logic with transmission gate logic to achieve high performance and energy efficiency. The research began with the development of a single-cycle operational model, which was later extended to a 32-bit architecture to evaluate scalability, timing behavior, and overall system performance under realistic computational workloads. All circuit designs were implemented and rigorously analyzed using Cadence Virtuoso, a leading EDA tool, across two key technology nodes: 180 nm and 90 nm. The primary focus was on three critical performance metrics — power consumption, propagation delay, and design area. These were systematically compared against several established full adder architectures, including complementary pass-transistor logic, transmission gate snake logic, transmission function snake logic, and hybrid pass-logic designs with static CMOS output stages. The objective was to identify configurations that deliver the best trade-offs between power efficiency, speed, and silicon area. At the 180 nm technology node, operating at a supply voltage of 1.8 V, the proposed full adder demonstrated outstanding results. It achieved an average power consumption of just 4.1563 µW while maintaining a very low propagation delay of 224 ps. This efficiency was realized through the strategic use of highly optimized CMOS inverter networks for low-power operation and carefully designed transmission gates to ensure reliable signal propagation with minimal energy dissipation. At the more advanced 90 nm technology node, operating at a reduced supply voltage of 1.2 V, the design exhibited even better performance. Power consumption dropped significantly to 1.17664 µW, and the propagation delay was reduced to only 91.3 ps. These improvements highlight the substantial benefits of technology scaling in achieving higher speed and lower energy requirements. When benchmarked against existing full adder designs, the proposed configurations consistently outperformed conventional approaches in terms of power efficiency and computational speed. The innovative integration of hybrid logic elements, combined with meticulous optimization at both circuit and architectural levels, enabled the designs to surpass previously reported benchmarks. This research contributes valuable insights into the design of high-performance, energy-efficient arithmetic circuits. The findings provide a strong foundation for future work aimed at further optimizing full adders and other arithmetic building blocks for next-generation digital systems, including processors, digital signal processors, and low-power embedded applications.

Index Terms— *Carry propagation adder, high speed, hybrid design, low power.*

1. Introduction

VLSI signifies "Incredibly Large Scale Integration". This is the field that incorporates squeezing progressively more reasoning contraptions into progressively little areas. VLSI, circuits that would have taken boards of space can now be put into a little space relatively few millimeters across! This has opened up a significant entryway to do things that were illogical beforehand. VLSI circuits are everywhere your PC, your vehicle, your crisp out of the plastic new state-of-the-art progressed camera, the cells, and what have you. This remembers a lot of expertise for some fronts inside the comparative field, which we will look at in later regions. VLSI has been around for a long time, but because of advances in the domain of PCs, there has been a shocking increase in devices that can be used to arrange VLSI circuits. Nearby, consenting to Moore's guideline, the limit of an IC has extended drastically all through the long haul, to the extent that estimation power, utilization of available area, yield. The united effect of these two advances is that people can now put different helpfulness into the Ic's, opening up new edges. Models are introduced systems, where brilliant contraptions are

put inside conventional things, and ubiquitous figuring where little enrolling devices duplicate such a lot of that even the shoes you wear may truly achieve something accommodating like noticing your heartbeats. Consolidated circuit (IC) development is the engaging advancement for a whole host of innovative devices and systems that have changed the way wherein we live. Jack Kilby and Robert Noyce got the 2000 Nobel Prize in Physics for their formation of the organized circuit; without the consolidated circuit, neither semiconductors nor PCs would be anyway critical as they appear to be today. VLSI systems are significantly more humble and consume less power than the discrete parts used to develop electronic structures before the 1960s. Compromise licenses us to build systems with significantly more semiconductors, allowing considerably seriously handling capacity to be applied to handling an issue. Composed circuits are similarly significantly more direct to plan and deliver and are more strong than discrete systems; that makes it possible to encourage specific explanation structures that are more viable than extensively valuable PCs for the principle work.

Advantages Of Vlsi

While we will zero in on composing circuits in this book, the properties of consolidated circuits that we can and can't put in a fused circuit generally choose the plan of the entire system. Facilitated circuits further foster structure characteristics in a greater number of ways than one. I appreciate three basic high grounds over automated circuits worked from discrete parts:

• Size. Composed circuits are much more unobtrusive the two semiconductors and wires are contracted to micrometer sizes, standing out from the millimeter or centimeter sizes of discrete parts. Little size prompts benefits in speed and power use since more unobtrusive parts have more unassuming parasitic assurances, capacitances, and inductances.

• Speed. Signs can be traded between reasoning 0 and reasoning 1 a lot quicker inside a chip than they can between chips. Correspondence inside a chip can happen commonly faster than correspondence between chips on a printed circuit load up. The high speed of circuits on-chip is a result of their little size-more unassuming parts and wires have more humble parasitic capacitances to tone down the transmission.

• Power usage. Reasoning errands inside a chip similarly take extensively less power. Once lower power usage is generally a direct result of the little size of circuits on the chip-more unobtrusive parasitic capacitances and securities require less capacity to drive them.

Routing

The arranging framework picks the specific ways for interconnections. This merges the standard cell and gigantic expansion sticks, the pins on very far or pads past what many would think about conceivable. After a strategy and CTS, the instrument has information about the particular areas of squares, pins of squares, and I/O pads at chip limits. The expected relationship as portrayed by the netlist is furthermore open to the mechanical social affair. In the getting sorted out stage, metal and vias are used to make the electrical relationship in arrangement to complete all affiliations portrayed by the netlist. Now, to do the authentic interconnections, the contraption relies on some "Plan Rules".

Most of the switches open are network-based switches. There are arranging lattices portrayed for the entire course of action. Consider it as a plan as under. For structure-based switches, there are moreover preferred controlling headings portrayed for each metal layer. for instance, Metal1 has an inclined in the direction of the course of "level', metal2 has truly leaned toward coordinating heading of "vertical, and so on Along these lines, in the whole course of action, metal1 arranging affiliations will be drawn (superimposed) on a level plane with metal1 wire pitch and metal2 cross-regions will be drawn vertical with metal2 wire pitch between each.

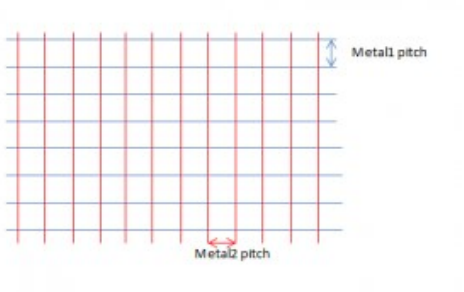

Figure 1 : Routing Grids

The above figure shows how coordinating grids are drawn. Here only two metals are considered for the present, but in a cycle with more metals, relative structures will be superimposed on the organization for each available metal. Not entirely settled by concluding the base scattering expected between system lines of the same metal.

This can be the base scattering of the metal but is by and large a value more imperative than the base isolating. Not set in stone by considering the through viewpoint additionally, with the objective that no two connecting wires on the cross-section make any DRC encroachment regardless when there are vias present.

2. Experience and Assessment:

Our transitory work range was of a half year. Immediately when we started, classes were coordinated and I acquired various thoughts as indicated by present-day viewpoint and liked them executing all things considered. Then, our affiliation had embraced projects from St. Mary's school, Hyderabad, a piece of those errands were done by me and I went to the show in that school and connected with students for our affiliation.

The inclusion with the association was pleasant, people work in co-arrangement and the association environment is especially safeguarded and studios. The inspiration to pick this association was that it was offering section level situation in VLSI which is my middle specialization in PG degree and I expected to benefit from this experience, in like manner I got to learn new instruments like Electric, Symica DE, and Microwind.

I used to spend just about 5 to 6 hours consistently in the association offering a chance with different circuits and making their arrangements genuinely. I thank my helper who was, by and large, there nearby all through my brief work process offering me direction, information, and tips on how people work in an industrial environment.

3. Low Power-Area Efficient Design of 1 cycle Full Adder:

In the nanometer setup plan, spillage power has a major need of complete power. The use of power has been extended as in a general sense significant in the piece of the plan for each Integrated Circuits(IC). On an extra note is a significant number of shuffling movements are used occasionally in a colossal degree as well as extraordinarily enormous extension blend application arranged DSP and central processor plans. The Full snake circuit arrangement is especially crucial and to be a certain unit of an ALU, which picks the structure's overall direction. The power use of a processor depends upon the ALU, so the power consumed by the full snake circuit in the ALU should get somewhat decreased to facilitate the necessities of an organizer in this way it will be called "a less filled arrangement".

4. Some of the Conventional Full Adder Designs

The low power full snake plans have been arranged and done by various XOR and XNOR modules. The reasoning of DOMINO and PTL drives the organizer to design a full snake with low power and deferment. In the full snake plan thoughts, the SERF (Static energy recovery Adder) plan and GDI (Gate Diffusion Input) techniques were ordinary. To diminish the power fairly the Pseudo NMOS reasoning is used with an inverter. To make the outcome that is the pass in faster mean and on to diminish power concede thing the sub edge 1-bit full snake and combination CMOS styles have been used. The proposed arrangement will be under Pass semiconductor reasoning and the benefit of using PTL is its quick movement since it has less center capacitance. As the amount of semiconductors is lessened the power scattering is less and the effects of interconnection are particularly low however it in like manner consumes less area.

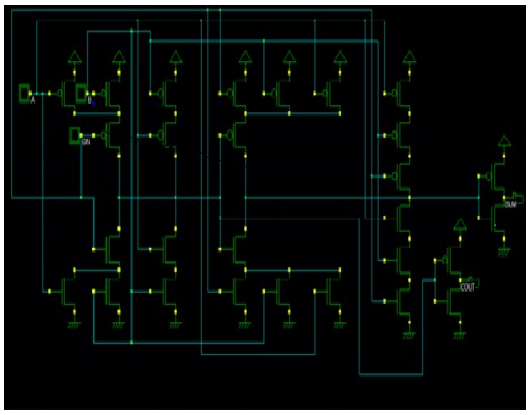

Figure 2: Schematic of Conventional Full Adder.

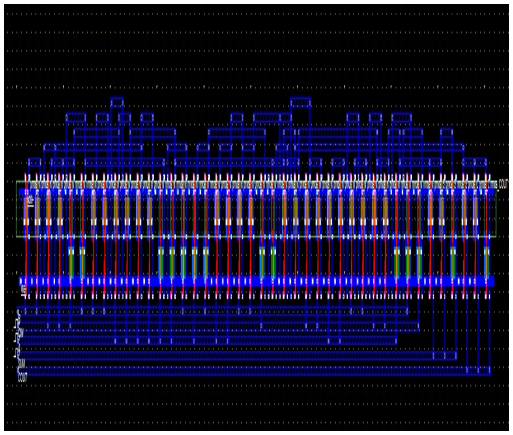

Figure 3: Layout of Conventional Full Adder.

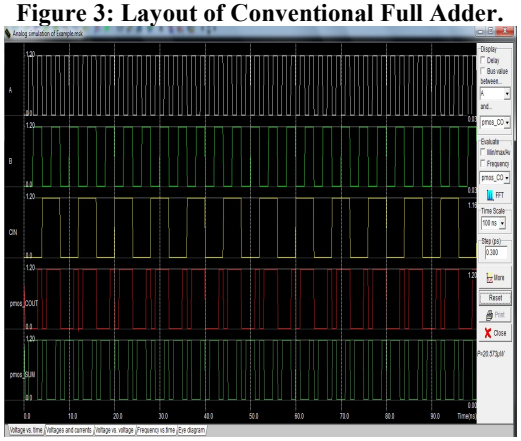

Figure 4: Layout Simulation of Conventional Full Adder.

In this section, several different designs of low power and high speed adders are introduced. The Static recovery adder(Figure 4) is the extreme low power design because in this design there will be direct contact path between supply and ground terminal and it also can re-apply the load charge to

the gate terminal as control(energy recovery)Figure 4.

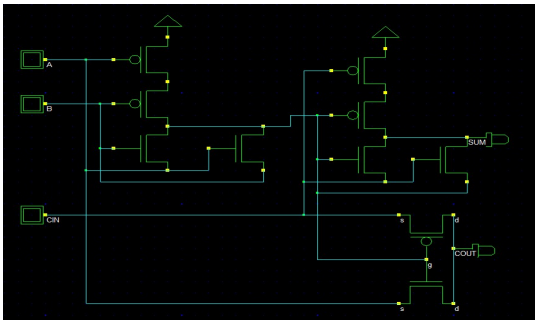

Figure 5: Schematic of SERF.

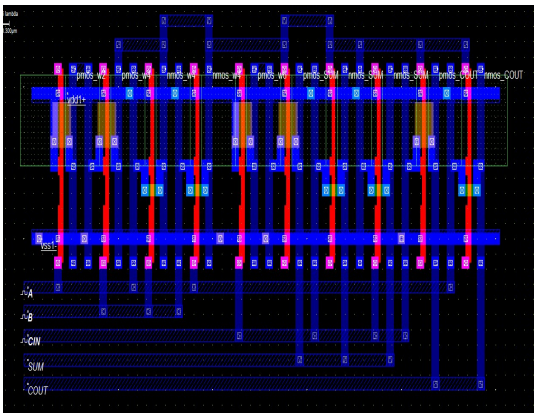

Figure 6: Layout of SERF.

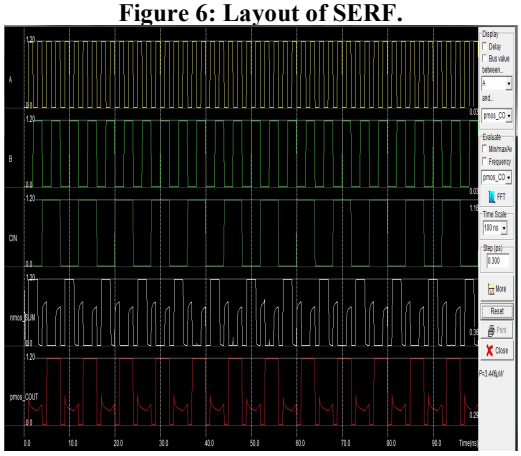

Figure 7: Layout Simulation of SERF.

Chowdhryet al. proposed a novel 8T full adder circuit shown in figure 7.

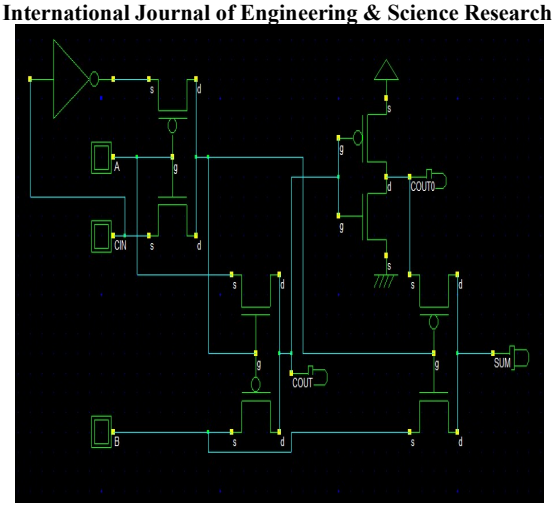

Figure 8; T Full Adder design

The low voltage operation, high computation speed and low delay degradation have been attained by using complementary and carry restoring logic.

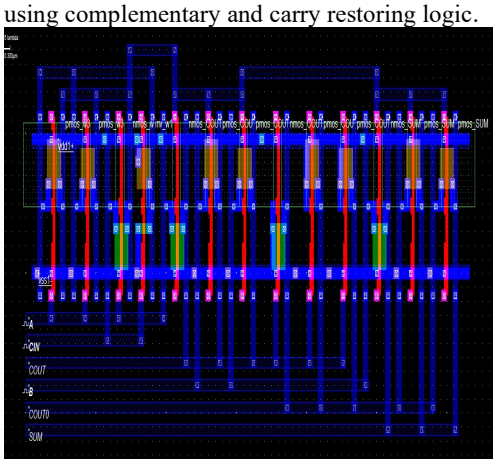

Figure 9: Layout of 8T Full Adder.

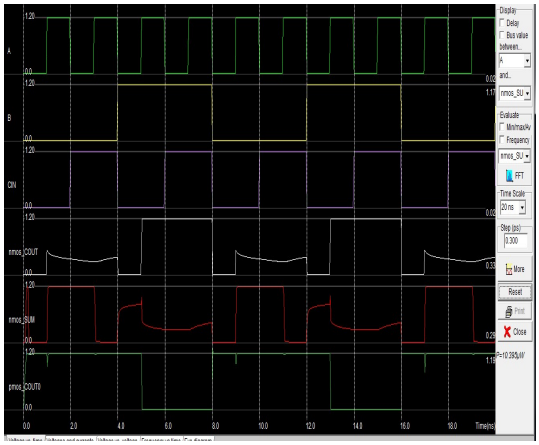

Figure 10: Layout Simulation of 8T Full Adder.

The design adopts inverter buffered XOR/XNOR designs to console the threshold voltage loss problem. However, most of the Pass transistor logic commonly causes two main problems. First one is that, slow operation at reduced voltages due to the threshold drop across the single-channel pass

transistors. It also reduces the current drive, since it is desirable to operate at very low possible operating voltage level which is specifically for the low power design.

Secondly, since the "high" input voltage level is not at the regenerative inverters, the inverter's PMOS is not fully turned off, so the direct-path static power dissipation could be significant. So I have designed a new full adder circuit consisting maximum of 6T which is analyzed and compared with earlier technique adder circuits.

4.1 Design of 6T Full Adder Circuit

The full adders of various designs of less transistor count will be in use of 3- module implementations that is XOR or XNOR for both sum as well as carry generating modules.

This full adder design is of low powered and transistors of less count which is verified using Microwind simulations. The circuit design is of 6T and with pass transistor logic. The power of this circuit is tremendously less when compared to the conventionally designed adder circuit which is of 28T and 8T static and energy recovery full adder (SERF) design, whereas the delay is comparatively less.

The design of PTL based technique will be required 4 transistors in least to design a XOR or XNOR model, but this design results in extreme threshold voltage loss problems. The main concern of this design is to use the Tristate inverter in the place of normal inverter which have been used for all low power designed circuits, because of the power consumption of the tri state inverter is less compared to normal one. This results in low operation throughput and average leakage of the circuit. Normally the inverter's supply voltage is HIGH always; whereas in Tristate inverter the supply voltage is not always HIGH. This reduces the operation throughput and average leakage of the circuit. Figure 10 shows the Tristate inverter.

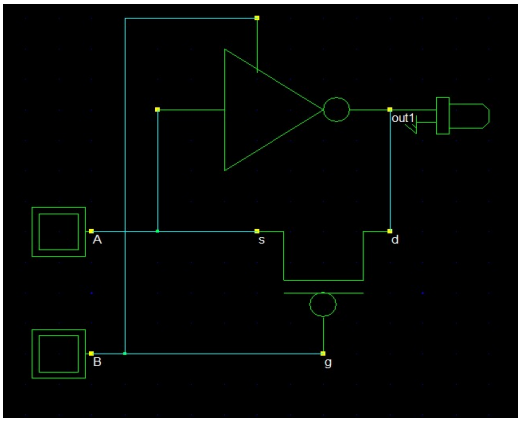

Figure 11: 3T XOR module

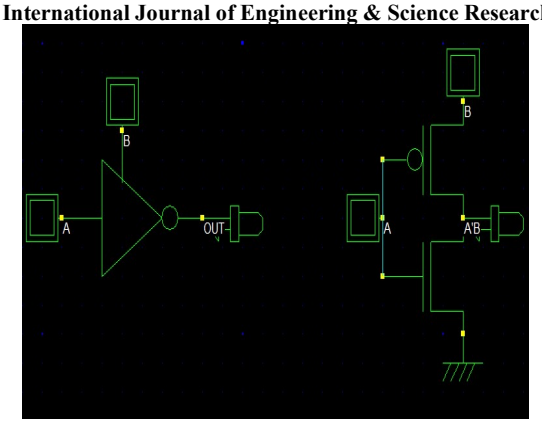

Figure 12: Tristate inverter

4.2 Proposed 6T full adder design

In the proposed 6T full adder sum is generated using 2 transistor XOR module twice, PMOS and NMOS is used to generate the carry. The below equations for Proposed 6T are,

Sum = (a xor b) xor c

⇨ (a xor b) c' + (a xor b)'c

Carry = ab + bc + ca

⇨ (a xor b)'a + (a xor b)c

In this design (a XOR b) signal is passed to the pass transistor based multiplexer made of two transistors to choose one among two signals. To generate carry (a XOR b) is sent to multiplexer to choose between a, c and to generate sum (a XOR a) is sent to choose between c', c. This simulation results comparatively less power consumption than the earlier designs whereas it is also used in Arithmetic and logic unit design.

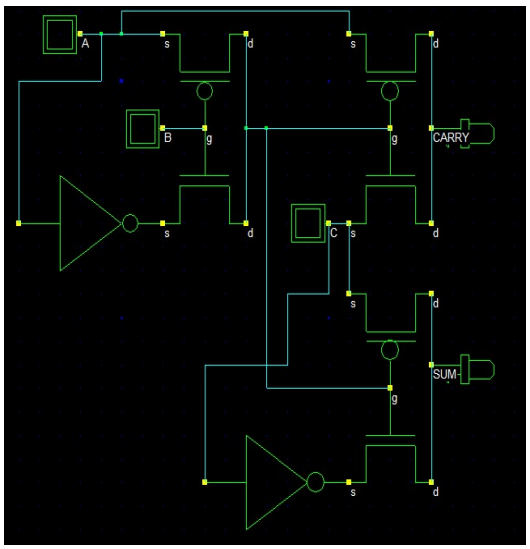

Figure 13; Proposed 6T Full Adder.

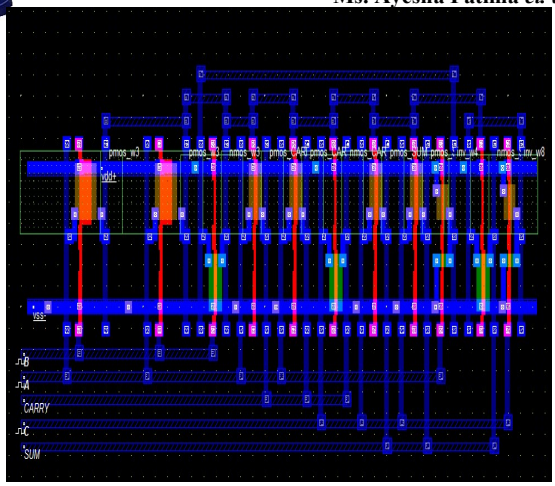

Figure 14; Layout of Proposed 6T Adder

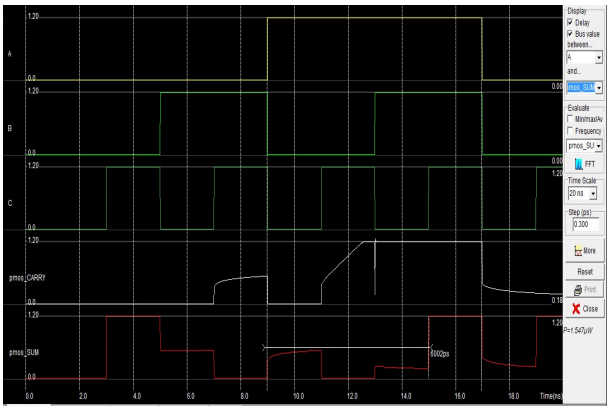

Figure 15; Layout Simulation of Proposed 6T Adder.

5. Result and Comparison

The entire simulations have been done on Microwind 2 for the power estimation and the consolidated results are compared with different techniques. The area is reduced tremendously when compared to 28T conventional full adder and SERF adder design.

Table 1 Simulation Results

Full adder designs	Conventional 28T	Chowdery et all (8T)	SERF	Proposed 6T
Average power consumption	22.569µW	10.453 µW	3.984 µW	1.547 µW
No. of transistors	28	8	10	6

6. Conclusion and Future Work

Simulation results obtained using Microwind 2 clearly demonstrate the effectiveness of the proposed 6T full adder design. The circuit exhibits significantly lower power consumption compared to both the conventional 28-transistor static CMOS full adder and the 10-transistor SERF (Static Energy Recovery Full Adder) design. This substantial reduction in energy dissipation highlights the potential of the proposed architecture for low-power VLSI applications, particularly in battery-operated portable devices and energy-constrained embedded systems.

In addition to improved power efficiency, the design maintains excellent signal integrity, with minimal output corruption observed across various operating conditions. This balance of low power and reliable performance further validates the practical viability of the 6T topology.

Implementation on Cadence Virtuoso

The next phase of development involves implementing and optimizing the 6T full adder on the **Cadence Virtuoso** platform. As a professional-grade EDA tool widely used in the semiconductor industry, Virtuoso will enable more detailed analysis, layout optimization, and performance refinement of the design. This step is expected to further enhance the circuit's characteristics and prepare it for integration into larger systems.

The proposed full adder also shows strong potential for practical application in more complex arithmetic circuits. Specifically, it can be effectively utilized in the Modified Booth Multiplier for efficient multiplicand encoding as well as in divider architectures, thereby extending its utility beyond standalone adders to broader computational units.

Value of the Microwind VLSI Design Tool

The use of Microwind during the internship proved highly beneficial. Its intuitive interface, powerful simulation capabilities, and comprehensive verification features made it an excellent platform for exploring and validating digital IC designs. The hands-on experience gained with this tool has strengthened technical proficiency and provided a solid foundation for future VLSI projects.

Personal and Professional Growth

Beyond technical skills, the internship offered substantial opportunities for personal and professional development. Collaborating with experienced professionals enhanced communication, teamwork, and problem-solving abilities. Working under expert guidance helped bridge the gap between academic knowledge and real-world industrial practices, while aligning with the organization's values fostered a deeper understanding of professional ethics and industry standards.

Overall, this internship has been a highly rewarding experience, combining meaningful technical contributions in low-power VLSI design with valuable personal growth. The practical exposure to industry tools and methodologies, along with the

successful development of the 6T full adder, has significantly strengthened both technical expertise and professional readiness for future roles in the semiconductor and digital systems domain.

References

1) **Mohammad Iliyas, A. Kumar, B. Reddy**, *Multi Stage Encoding Methods in Digital VLSI Circuits*, IJMETMR, Vol. 1, Issue 11, pp. 510–514, Nov. 2014.
2) **Mohammad Iliyas, Farha Anjum, Anil Kumar Sharma, R. Murali Prasad**, *Development of Low Power Test Data Compression Techniques for Digital VLSI Circuits*, IJARCCE, Vol. 5, Issue 12, pp. 423–425, Dec. 2016.
3) **Dr. Mohammad Iliyas et al.**, *Multi Stage Encoding Methods in Digital VLSI Circuits*, IJMETMR, Vol. 1, Issue 11, pp. 510–514, Nov. 2014.
4) **Dr. Mohammad Iliyas et al.**, *Code Based Compression Techniques in Digital VLSI*, IJMETMR, Vol. 2, Issue 10, pp. 1413–1419, Oct. 2015.
5) **Dr. Mohammad Iliyas et al.**, *Different Types of Data Compression Techniques in Digital VLSI Circuits*, IJMETMR, Vol. 3, Issue 2, pp. 1141–1145, Feb. 2016.
6) **Mohammed Imran, Dr. Amairullah Khan Lodhi, Dr. Mohammad Iliyas**, *Analyzing the Performance of a Hybrid 1-Bit Full Adder Circuit with Low Power Consumption and High Speed*, International Journal of Multidisciplinary Engineering in Current Research (IJMEC), Vol. 8, Issue 10, pp. 23–34, October 2023.
7) **Muzaffar Ali Mohammad, Rajesh Reddy Gade, Dr. Mohammad Iliyas**, *IoT-Based Security Applications for Industrial Automation: Enhancing Safety and Protection*, International Journal of Multidisciplinary Engineering in Current Research (IJMEC), Vol. 8, Issue 10, October 2023. *(Author list verified from the journal issue.)*
8) **Md. Akheel, E. Mahesh, Dr. Mohammad Iliyas**, *Design an Efficient 8-4 and 9-4 Compressors Optimized for High-Speed Multiplication*, International Journal of Multidisciplinary Engineering in Current Research (IJMEC), October 2023. *(This corresponds to the publication you listed as "High Speed Multiplier Design Using Optimized 8-4 and 9-4 Compressor Structures.")*
9) **Ms. Ayesha Mubeen, Dr. Mohammad Iliyas, Ms. Rubeena Begum**, *Optimizing CMOS Multiplexer Layout Design and Implementation Across Multiple Technologies*, International Journal of Multidisciplinary Engineering in Current Research (IJMEC), Vol. 9, No. 9, pp. 47–53, September 2024.
10) **Dr. Amariullah Khan Lodhi, Mrs. Hazira Siddiqui, Dr. Mohammad Iliyas**, *Comprehensive Analysis of Low Power Consumption and High-Speed Performance in a Hybrid 1-Bit Full Adder Circuit for Efficient Digital Processing*, International Journal of Multidisciplinary Engineering in Current Research (IJMEC), Vol. 9, No. 12, pp. 11–20, December 2024.

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