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Low power CMOS Op-Amp for IoT and Biomedical Applications

Ms Kazi Nikhat Parvin M[1], Kondla Bhavana[2], Bhukya Divya[3], Dannaram Manisha[4], Vadthya Anitha[5]
[1]Associate Professor; Department of Electronics and Communication Engineering, Bhoj Reddy Engineering College for Women Hyderabad India
[2,3,4,5]B.Tech students; Department of Electronics and Communication Engineering, Bhoj Reddy Engineering College for Women Hyderabad India
Mail Id; Manishareddymanisha999@gmail.com[4]
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Abstract
Energy-efficient analog circuit design has become increasingly important due to the rapid growth of Internet of Things (IoT) devices and biomedical monitoring systems. These systems typically operate using limited battery resources and must process extremely weak sensor signals. Therefore, operational amplifiers used in such applications must provide adequate gain and stability while consuming minimal power. This work presents the design of a low-power CMOS operational amplifier intended for IoT and biomedical signal conditioning applications.The proposed amplifier architecture employs a CMOS differential input stage combined with current mirror biasing and a gain stage to achieve efficient signal amplification under low supply voltage conditions. The design focuses on reducing bias currents in order to minimize overall power dissipation without significantly affecting amplifier performance. Such characteristics make the circuit suitable for portable, wearable, and implantable electronic devices.Operational amplifiers are essential in amplifying small bio-signals generated by sensors such as electrocardiogram (ECG), electroencephalogram (EEG), and electromyogram (EMG) sensors, as well as in sensor interface circuits commonly used in IoT systems. The designed amplifier provides reliable amplification of low-level signals while maintaining stability and sufficient bandwidth for low-frequency applications.The circuit design and performance evaluation were carried out using Cadence Virtuoso simulation tools. Simulation results confirm that the proposed CMOS operational amplifier achieves low power consumption while maintaining satisfactory voltage gain, bandwidth, and stability. These characteristics demonstrate the suitability of the design for energy-constrained biomedical instruments and IoT sensor interfaces. The proposed approach contributes to improved battery life and reliable signal processing in next-generation low-power electronic systems.
Keywords
Low-Power CMOS Amplifier, Operational Amplifier, IoT Systems, Biomedical Signal Processing, Low-Voltage Design, Cadence Virtuoso, Analog Integrated Circuits, Sensor Interface Circuits

Introduction
Recent technological developments have significantly increased the use of Internet of Things (IoT) devices and biomedical monitoring systems in modern electronic applications. These systems rely on various sensors to capture physiological and environmental data in real time, including signals such as heart rate, electrocardiogram (ECG), electroencephalogram (EEG), and electromyogram (EMG). However, the electrical signals generated by such sensors are typically very small in magnitude and highly sensitive to noise and interference. As a result, accurate amplification and conditioning of these signals are essential for reliable data acquisition and processing.
The operational amplifier (Op-Amp) is a fundamental component in analog and mixed-signal integrated circuits and is widely used in signal amplification, filtering, data acquisition, and analog signal conditioning. In IoT and biomedical systems, operational amplifiers are commonly integrated into sensor interfaces, analog front-end circuits, monitoring devices, and data conversion systems. Despite their importance, traditional operational amplifier designs often consume relatively high power, which limits their suitability for battery-powered and portable electronic devices.IoT nodes and biomedical monitoring systems are typically required to operate for extended periods using limited energy sources such as batteries or energy harvesting units. Consequently, minimizing power consumption has become a critical design requirement in these applications. In addition to low power operation, amplifiers used in such systems must also provide sufficient voltage gain, stable operation, low noise performance, and reliable functionality under low supply voltage conditions. These challenges have driven significant research efforts toward the development of low-power CMOS operational amplifier architectures.Complementary Metal-Oxide-Semiconductor (CMOS) technology is widely adopted for low-power analog circuit design due to its inherent advantages, including low static power

dissipation, high integration capability, and compatibility with modern semiconductor manufacturing processes. By carefully optimizing transistor sizing, biasing strategies, and frequency compensation techniques, designers can achieve operational amplifiers that maintain acceptable performance while consuming minimal power.This work focuses on the design and simulation of a low-power CMOS operational amplifier intended for IoT sensor interfaces and biomedical instrumentation. The proposed design aims to achieve reduced power consumption while maintaining adequate gain, stability, and bandwidth suitable for processing low-frequency physiological signals.

Literature Survey

Several research efforts have addressed the challenges associated with designing low-power operational amplifiers for biomedical and IoT applications. Harrison and Charles (2003) presented a low-power and low-noise CMOS amplifier specifically developed for neural signal recording systems. Their design operated at a reduced supply voltage and consumed only micro-watt level power while maintaining low input-referred noise. To minimize flicker noise, the authors employed PMOS transistors in the input stage, which made the amplifier particularly suitable for processing low-frequency biomedical signals such as EEG and ECG.Xu and Zhang (2020) proposed an ultra-low-power CMOS operational amplifier targeted at IoT sensor nodes using a current-reuse technique. In this approach, the same bias current is shared across multiple amplifier stages, thereby significantly reducing overall power consumption. The amplifier operated at a supply voltage of approximately 1 V and consumed less than 2 µW of power. The study demonstrated that current-reuse architectures can effectively extend the operational lifetime of battery-powered IoT devices and energy-harvesting sensor systems.Enz and Temes (1996) investigated circuit techniques aimed at reducing the impact of operational amplifier imperfections, particularly low-frequency noise and offset voltage. Their work focused on the implementation of auto-zeroing and chopper stabilization methods in CMOS amplifiers. These techniques are particularly useful in biomedical instrumentation where signal amplitudes are extremely small and susceptible to noise. The study showed that chopper stabilization can significantly suppress 1/f noise and improve signal accuracy. However, the authors also noted that these techniques increase circuit complexity and may introduce additional power consumption due to switching components.

Joung and Lee (2018) explored adaptive biasing techniques for achieving ultra-low-power CMOS amplifier designs. In their approach, the bias current of the amplifier is dynamically adjusted depending on the input signal conditions. This adaptive behavior allows the amplifier to reduce power consumption during low activity periods while maintaining performance when higher signal levels are present. The proposed technique demonstrated improved power efficiency and provided a practical solution for energy-constrained analog circuits.

Operational Amplifier and CMOS Fundamentals

Operational amplifiers play a key role in modern electronic systems by providing accurate signal amplification and processing. An op-amp is essentially a differential amplifier that amplifies the voltage difference between two input terminals: the inverting input and the non-inverting input. Because of their versatility, operational amplifiers are widely used in signal processing applications such as voltage amplification, filtering, instrumentation, and data acquisition systems.In theoretical analysis, the operational amplifier is often modeled with ideal characteristics including infinite gain, infinite input impedance, zero output impedance, and zero offset voltage. However, practical implementations deviate from these assumptions due to the physical limitations of semiconductor devices. Real op-amps exhibit finite gain, limited bandwidth, input offset voltage, noise, and non-zero power consumption. Despite these limitations, advances in semiconductor fabrication technologies have enabled the development of high-performance operational amplifiers that closely approximate ideal behavior for many applications.CMOS technology is widely used in modern integrated circuit design because it employs complementary pairs of NMOS and PMOS transistors, which significantly reduce static power consumption. This characteristic makes CMOS circuits particularly suitable for portable and battery-powered devices. In CMOS operational amplifiers, MOS transistors are used to implement key circuit blocks such as differential input stages, current mirrors, gain stages, and output buffers.The MOSFET acts as the fundamental active device in CMOS circuits and operates as a voltage-controlled current source. By adjusting the gate-to-source voltage, the current flowing through the device can be controlled. MOS transistors operate in three primary regions: cut-off, triode, and saturation. For analog amplification purposes, transistors are typically biased in the saturation region, where stable gain and predictable behavior can be achieved. Proper biasing and careful transistor sizing are therefore essential to obtain the desired amplifier characteristics such as gain, bandwidth, and power efficiency.CMOS operational amplifiers are particularly advantageous in applications requiring low power consumption and low supply voltage operation. This makes them highly suitable for IoT sensor nodes and biomedical devices, where long battery life and reliable signal processing are critical. Biomedical signals are typically small in amplitude and low in frequency, which requires amplifiers with high input impedance and low noise characteristics. CMOS technology enables the implementation of such features while maintaining low power dissipation.

Need for Embedded Systems

The growing demand for portable and wearable electronic devices has increased the need for efficient low-power analog circuits. Embedded systems used in IoT networks and biomedical monitoring equipment frequently rely on operational amplifiers for sensor interfacing, signal conditioning, and data acquisition. Since these systems often operate continuously for extended periods using limited power sources, minimizing energy consumption is a major design requirement.Low-power CMOS operational amplifiers provide an effective solution for these applications by reducing overall system power dissipation while maintaining reliable performance. In IoT and biomedical systems, sensors generate weak analog signals that must be accurately amplified before digital processing can occur. CMOS technology supports the design of amplifiers that operate at low supply voltages while consuming minimal static power.Such characteristics make CMOS operational amplifiers ideal for applications including wearable health monitoring devices, implantable medical equipment, and distributed IoT sensor networks. Additionally, reducing power consumption helps minimize heat generation, which is particularly important in biomedical applications where device safety and patient comfort are essential. As a result, low-power CMOS amplifiers contribute significantly to improved reliability, longer battery life, and enhanced performance of embedded electronic systems.

Low Power CMOS Operational Amplifier Design

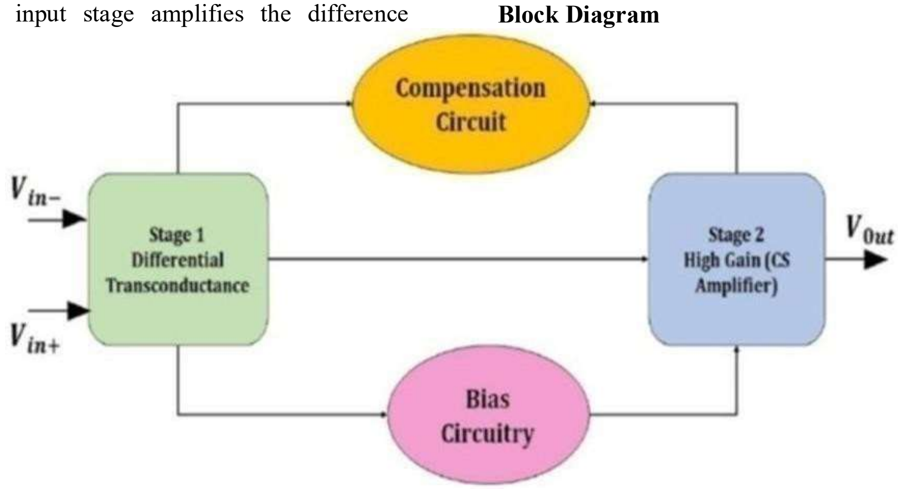
Conventional Operational Amplifier Design

Traditional operational amplifiers typically employ a multi-stage architecture to achieve high gain and stable operation. A common configuration includes three main stages: a differential input stage, a high-gain intermediate stage, and an output stage. The differential input stage amplifies the difference between the two input signals while rejecting common-mode noise. This stage also provides high input impedance, which is essential for accurate signal acquisition.The second stage, often called the gain stage, provides the majority of the amplifier's voltage gain. It is commonly implemented using a common-source amplifier with active loads. To ensure stability when feedback is applied, compensation techniques such as Miller compensation are introduced to control the frequency response of the amplifier.The output stage is responsible for driving the load and providing low output impedance. This stage allows the amplifier to deliver sufficient output current while preserving signal integrity. Although conventional designs offer high gain and good stability, they typically require higher supply voltages and consume more power. Therefore, modifications are necessary when designing amplifiers for low-power applications.

Proposed System

The proposed system focuses on designing a low-power CMOS operational amplifier intended for IoT and biomedical signal processing. The primary objective is to reduce power consumption while maintaining adequate gain, stability, and noise performance. CMOS technology is chosen because of its low static power dissipation and compatibility with low-voltage operation.The proposed amplifier architecture is designed to efficiently amplify weak signals generated by sensors in biomedical and IoT systems. By optimizing transistor sizing and bias currents, the amplifier achieves improved energy efficiency while maintaining reliable performance. This design approach addresses the limitations of conventional operational amplifiers that consume higher power in battery-operated environments.Key features of the proposed system include low power consumption, low-voltage operation, high input impedance, and improved noise performance. These characteristics make the amplifier suitable for wearable health monitoring devices, medical instrumentation, and IoT sensor interfaces.

Block Diagram



Block Diagram

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The operational amplifier architecture consists of several functional blocks that work together to achieve high gain and stable performance. The process begins with the differential input stage, where the input signals are applied to the inverting and non-inverting terminals. This stage amplifies the voltage difference between the two inputs while rejecting common-mode noise.The amplified signal is then converted into a current through the transconductance mechanism of the differential pair. This current signal is further amplified in the second stage, which provides most of the voltage gain. A compensation circuit is introduced between the first and second stages to control the frequency response and prevent oscillations during feedback operation.Bias circuitry provides the required operating currents and voltages for all amplifier stages, ensuring that the MOS transistors operate in the desired region. Finally, the output stage delivers the amplified signal to the load while maintaining low output impedance.

Methodology

The design methodology for the CMOS operational amplifier follows a systematic approach to achieve stable operation, sufficient gain, and low power consumption. Initially, a two-stage amplifier architecture is selected due to its ability to provide high gain with relatively simple design complexity. The first stage is a differential input stage that offers high input impedance and strong common-mode rejection capability.Next, a biasing network is designed to provide stable operating currents for all transistors. Proper biasing ensures that MOS devices remain in the saturation region, which is necessary for linear amplification. The second stage is implemented as a common-source amplifier that significantly increases the overall voltage gain.To maintain stable operation, frequency compensation techniques are introduced to control the amplifier's frequency response and ensure adequate phase margin. Finally, the output stage is designed to provide sufficient output swing and drive capability. After completing the circuit design, performance parameters such as voltage gain, bandwidth, power consumption, common-mode rejection ratio (CMRR), and power supply rejection ratio (PSRR) are evaluated through simulation.

CMOS Op-Amp Software Description

Cadence Design Tools

Cadence Virtuoso provides a comprehensive environment for analog circuit design and simulation. The Virtuoso Schematic Editor is used to create circuit schematics and define transistor dimensions required for low-power operation. The Analog Design Environment (ADE) allows designers to configure simulations and analyze circuit behavior under various operating conditions.The Spectre simulator serves as the core engine for performing accurate SPICE-level simulations. Additional tools within the Cadence platform enable layout design and verification. Layout verification is performed using Design Rule Checking (DRC) and Layout Versus Schematic (LVS) to ensure that the physical layout follows fabrication constraints and matches the original schematic.The Cadence log window provides important diagnostic information during simulation, including messages related to library loading, device model linking, and simulation initialization. This information assists designers in identifying potential errors and ensures that the simulation environment is properly configured.

Power Supply and Bias Conditions

The CMOS operational amplifier operates using a supply voltage selected according to the technology used for implementation. For low-power designs, a supply voltage around 1.8 V is commonly used. Proper biasing is achieved using current mirror circuits that generate stable bias currents for each amplifier stage.A tail current source is used to bias the differential input stage, while additional bias voltages are applied to current mirror transistors to establish appropriate operating points. DC operating point analysis ensures that all MOS transistors operate in the saturation region and maintain stable quiescent currents.

CMOS Differential Amplifier Stage

The differential amplifier forms the input stage of the CMOS operational amplifier and is responsible for providing high input impedance and rejecting common-mode noise. It is implemented using a matched pair of NMOS transistors with a constant current source acting as the tail current. PMOS transistors are used as active loads to improve voltage gain and reduce circuit area.

This configuration allows the differential stage to convert the input voltage difference into a current signal while maintaining stable biasing conditions. The stage also provides the initial amplification required for further signal processing in the following stages.

Chapter 5

Results and Discussion

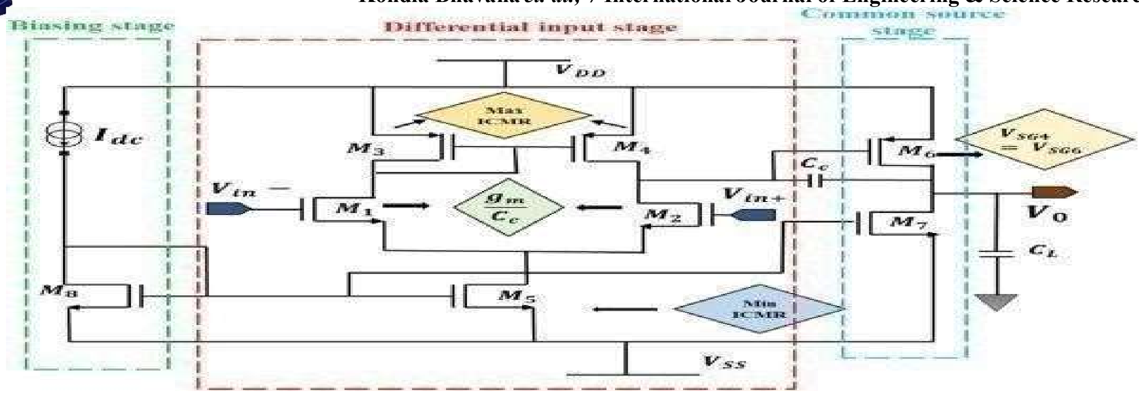

Fig 1 working of CMOS operational amplifier design for industrial

This chapter presents the simulation results and performance evaluation of the proposed low-power CMOS operational amplifier designed for Internet of Things (IoT) and biomedical applications. The circuit was implemented and simulated using the Cadence Virtuoso design environment with a 180 nm CMOS technology model. Various analyses, including AC analysis, transient analysis, and layout verification, were performed to evaluate the operational characteristics of the amplifier. The obtained results demonstrate the amplifier's capability to provide adequate gain, bandwidth, and stability while maintaining low power consumption.

Working and Performance Evaluation

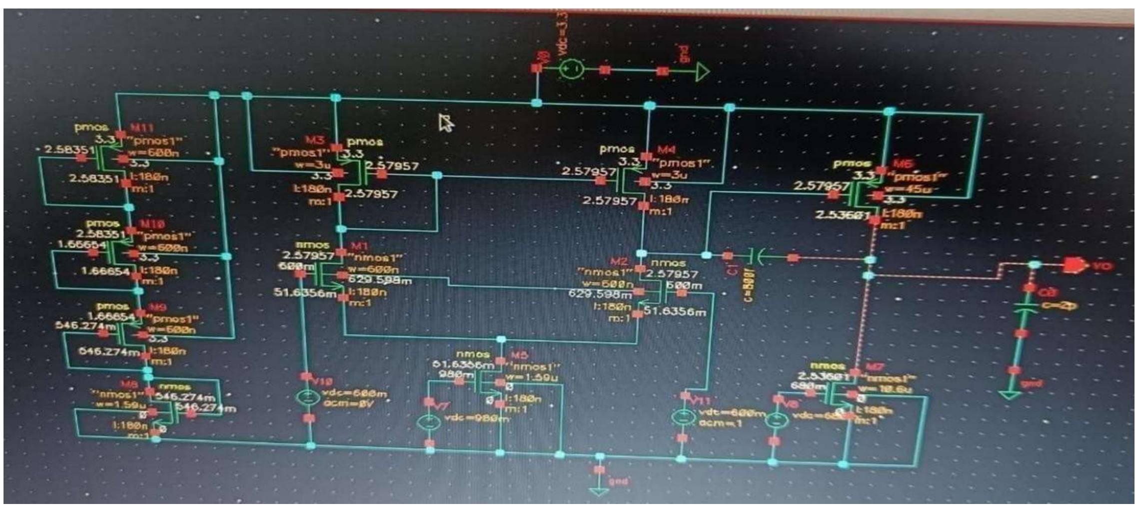

Fig 2 CMOS operational amplifier (Op-Amp) with a two-stage schematic design utilising 180 nm technology.

The designed CMOS operational amplifier was simulated using Cadence analog design tools to analyze its performance under different operating conditions. The simulation environment utilized a 180 nm CMOS technology model to accurately represent transistor behavior. The proposed amplifier employs an active load configuration, which improves gain and reduces power consumption compared to traditional current-source biased architectures.Simulation results show that the amplifier achieves a slew rate of approximately 20.7 V/µs and a power supply rejection ratio (PSRR) of about 179.45 dB under ideal operating conditions. Both transient and AC analyses were performed to evaluate time-domain and frequency-domain characteristics. When an input signal of approximately 600 mV was applied, the output voltage reached around 1.709 V, demonstrating effective signal amplification.AC analysis was conducted over a wide frequency range from 100 Hz to 10 GHz to observe the variation in output response with frequency. The results indicate that the amplifier maintains strong gain at low frequencies and gradually decreases as the frequency increases due to internal parasitic capacitances. Process, voltage, and temperature (PVT) variations were also simulated to verify the robustness of the design across different operating conditions. The analysis confirmed stable operation across temperature ranges from −80 °C to 100 °C.Monte-Carlo simulations using the Cadence ADE XL environment were performed to evaluate the effect of device mismatch and process variations. The results indicated that the proposed amplifier achieves a minimum DC gain of approximately 59.09 dB across all simulated conditions. At nominal operating conditions and a supply voltage of 3.3 V, the amplifier demonstrated a maximum gain of approximately 62.94 dB with a phase margin of about 60.13°, indicating stable operation.Compared with earlier designs that used current source biasing, the proposed design demonstrates improved performance. The conventional amplifier achieved a gain of about 62.49 dB, a CMRR of 67.80 dB, and power dissipation of approximately 808 µW. In contrast, the proposed design with an active load implementation achieves a gain of approximately 62.94 dB, a significantly higher CMRR of about 92.80 dB, and reduced power consumption of approximately 234 µW. These results confirm that the proposed architecture provides better noise rejection and improved energy efficiency.Furthermore, the proposed design requires only 11 transistors, whereas conventional implementations typically require between 11 and 32 transistors. This reduction in transistor count contributes to a more compact circuit layout and improved integration density. The layout area of the proposed amplifier is approximately 0.001476 mm², which is significantly smaller than many previously reported designs.

Schematic Design

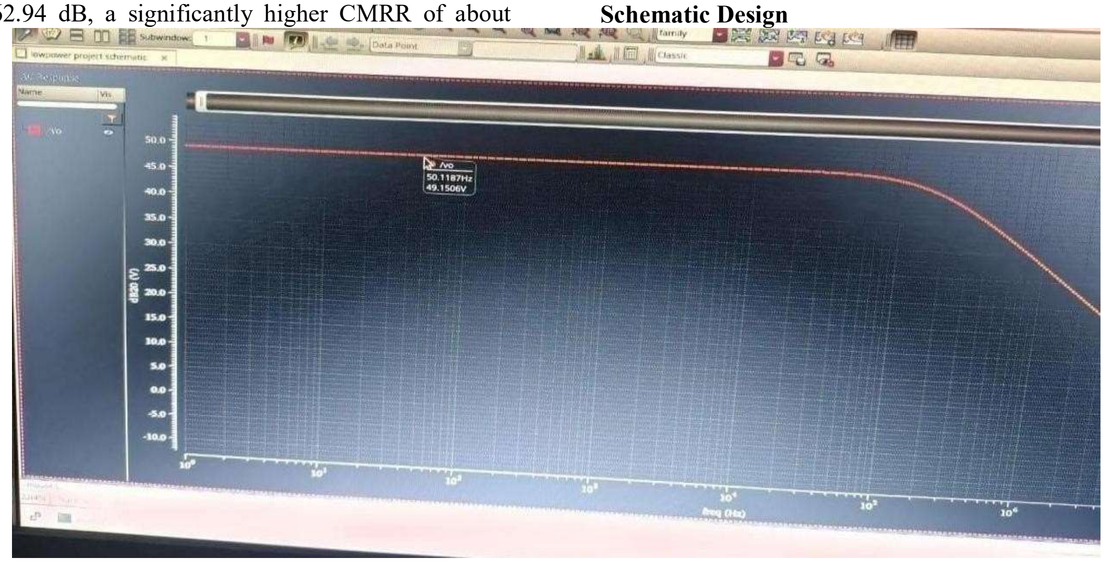

Fig 3 Gain Analysis of CMOS Op-Amp Using 180nm

The schematic of the two-stage CMOS operational amplifier was implemented using the Cadence Virtuoso schematic editor with a 180 nm technology library. The amplifier consists of three primary sections: a differential input stage, a second gain stage, and a biasing network. The differential input stage is responsible for amplifying the voltage difference between the two input terminals. Matched NMOS transistors are used to form the differential pair, while PMOS current mirror loads convert the differential signal into a single-ended output.The second stage acts as a common-source amplifier and provides additional voltage gain to the signal generated by the input stage. A Miller compensation capacitor is connected between the first and second stages to ensure stable frequency response and prevent oscillations during feedback operation. The biasing network uses current mirror structures to generate constant bias currents required for stable operation.

Gain Analysis

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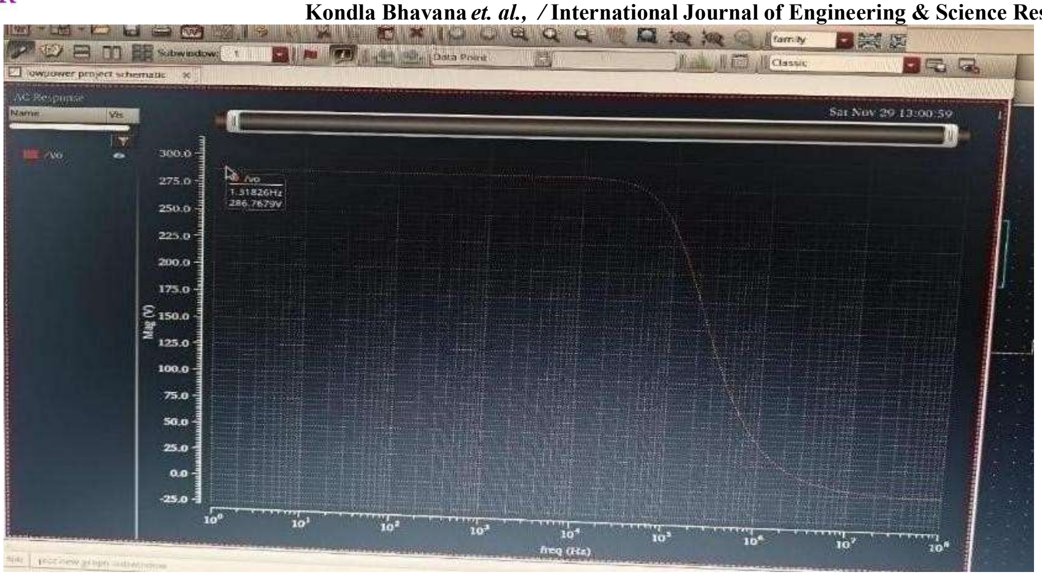

Fig 4 A.C Analysis of CMOS Op-Amp Using 180nm

Frequency response analysis was performed to determine the gain characteristics of the amplifier. The Bode magnitude plot shows that the amplifier maintains a nearly constant gain at low frequencies, representing the midband region. The midband gain was measured at approximately 49.15 dB, which corresponds to a linear gain of about 286 V/V. As frequency increases, the gain gradually decreases due to parasitic capacitances present within the circuit. This behavior is typical of practical operational amplifiers and indicates a low-pass filter characteristic

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AC Analysis

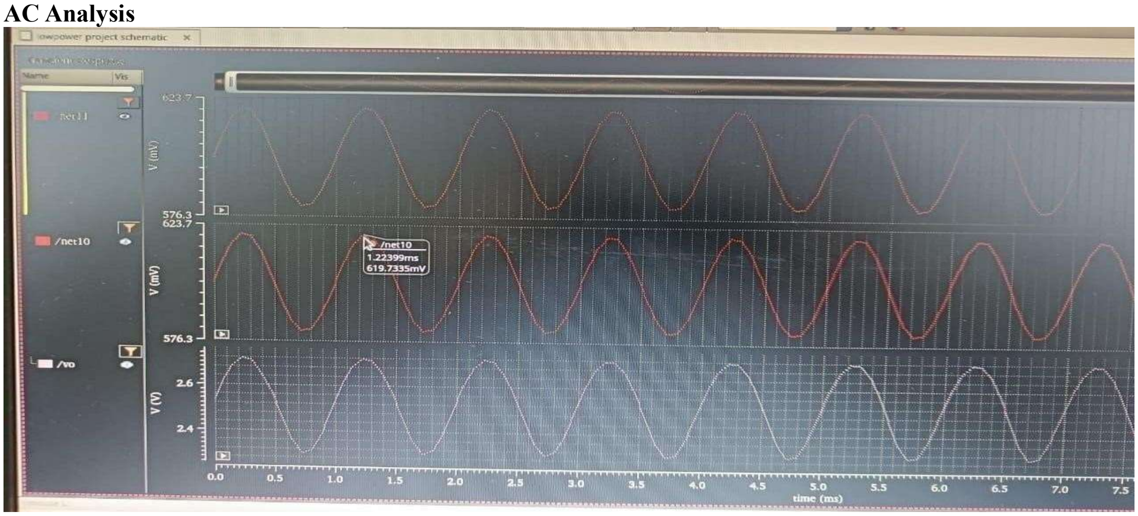

Fig 5 A Transient analysis of the CMOS Op-Amp utilising 180 nm Technology.

AC analysis was conducted to evaluate the amplifier's frequency response and bandwidth. The gain remains relatively constant at low frequencies, indicating stable amplification. As the frequency approaches higher values, the gain decreases due to the presence of internal poles in the amplifier. The −3 dB cutoff frequency was observed between approximately 200 kHz and 250 kHz, defining the effective bandwidth of the amplifier.The gain-bandwidth behavior confirms that the proposed amplifier can effectively amplify low-frequency signals, which are common in biomedical and sensor-based applications.

Transient Analysis

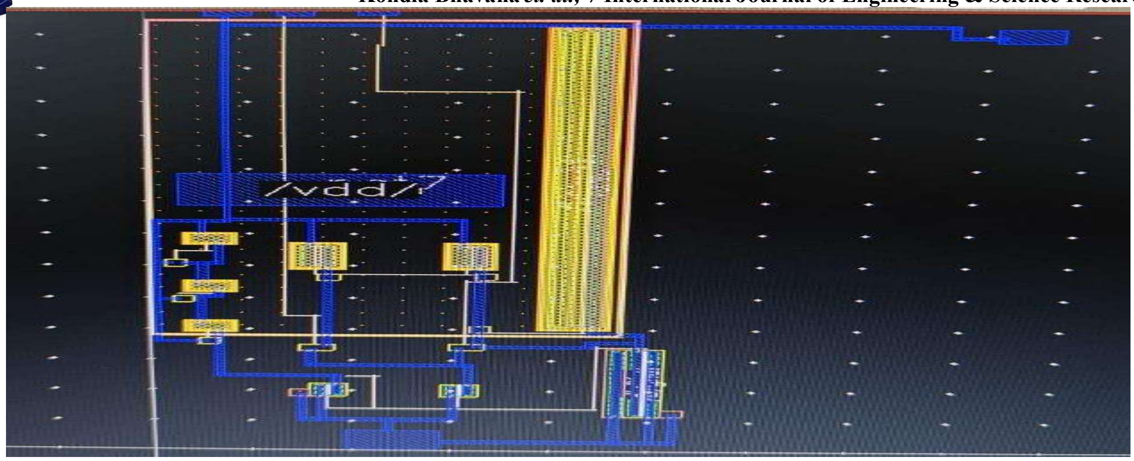

Fig 6 Layout of Low Power CMOS Op-Amp.

Transient analysis was performed to examine the time-domain response of the amplifier. The simulation shows sinusoidal input signals with small amplitudes around 600 mV, while the output waveform exhibits a significantly larger amplitude between approximately 2.3 V and 2.7 V. This confirms that the circuit successfully amplifies the input signal while maintaining stable operation.The transient gain was calculated using the ratio of output voltage to input voltage, resulting in an approximate gain of 4 V/V in the time domain. The slew rate was determined using the change in output voltage over time and was calculated as approximately 0.0008 V/µs. This value lies within the typical range required for biomedical signal processing, where signal variations occur slowly.

Layout Implementation

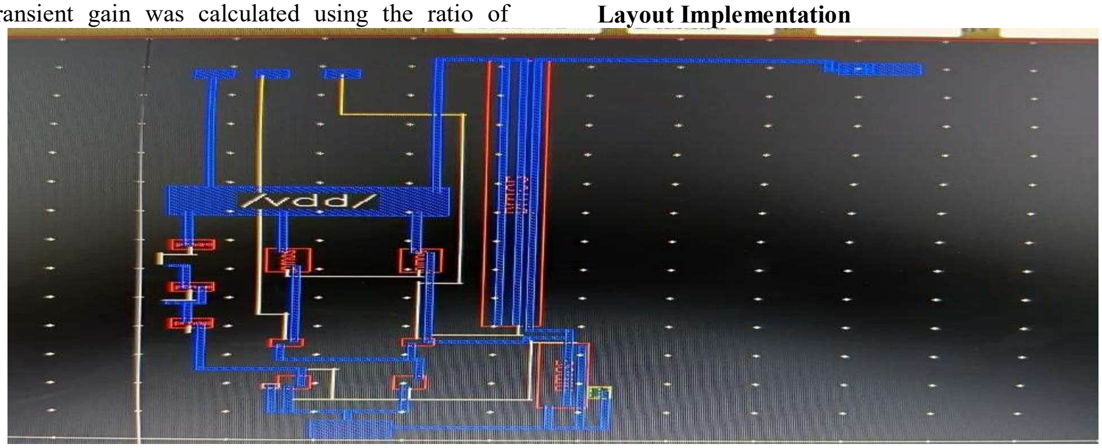

Fig 7 CMOS Operational Amplifier Layout showing VDD routing, transistor placement, and interconnections designed using Cadence Virtuoso

The physical layout of the CMOS operational amplifier was designed using the Cadence Virtuoso layout editor. The layout includes various fabrication layers such as diffusion regions, polysilicon gates, metal interconnections, and contacts. PMOS transistors are placed within the N-well region near the VDD power rail, while NMOS transistors are located in the lower section connected to ground.Careful attention was given to transistor matching and symmetrical placement, particularly for the differential input pair. This layout strategy helps minimize mismatch errors and improve overall circuit accuracy. Multiple contacts and metal routing layers were used to ensure reliable electrical connectivity and reduce parasitic resistance.The complete layout occupies an area of approximately 67.325 µm × 29.61 µm (≈1993.5 µm²). Design Rule Checking (DRC) was performed successfully, confirming that the layout satisfies all fabrication constraints. Layout Versus Schematic (LVS) verification was also performed to ensure that the physical implementation matches the schematic design.

Applications

Low-power CMOS operational amplifiers have a wide range of applications in modern electronic systems due to their energy efficiency and compact design. In biomedical wearable devices, these amplifiers are used to process physiological signals obtained from sensors such as ECG, EEG, and EMG. The ability to amplify very small signals while maintaining low noise makes them suitable for medical monitoring systems.In IoT sensor interfaces, operational amplifiers play an important role in conditioning signals from environmental sensors that measure temperature, pressure, humidity, or gas concentration. These amplified signals can then be processed by digital controllers for smart city and industrial monitoring applications.Portable consumer electronics such as smartwatches, fitness trackers, and portable audio devices also rely on low-power operational amplifiers for analog signal processing. Implantable medical devices, including pacemakers and neural stimulators, require extremely energy-efficient amplifiers to minimize heat generation and extend battery life.Additionally, these amplifiers are useful in energy harvesting systems where circuits operate using extremely limited power sources such as solar or thermal energy. Wireless sensor networks also benefit from low-power operational amplifiers because reduced power consumption increases the operational lifetime of distributed sensor nodes.

Conclusion

In this work, a two-stage CMOS operational amplifier was successfully designed and analyzed using 180 nm CMOS technology. The amplifier was implemented and simulated using Cadence Virtuoso tools, enabling detailed evaluation of its electrical performance. The results obtained from AC analysis indicate a midband gain of approximately 49.15 dB, corresponding to a linear gain of about 286 V/V. The −3 dB cutoff frequency was observed between 200 kHz and 250 kHz, defining the effective bandwidth of the amplifier.Transient analysis confirmed correct time-domain operation with a calculated slew rate of approximately 0.0008 V/μs. This performance is suitable for low-frequency signal processing applications commonly found in biomedical instrumentation.The physical layout of the amplifier was also implemented and verified using design rule checking. The layout occupies a compact area of 67.325 μm × 29.61 μm and satisfies fabrication requirements. The project successfully demonstrates the complete analog integrated circuit design process, including schematic design, simulation, layout implementation, and verification.

Future Scope

Future research in CMOS operational amplifier design will focus on several important directions. Advanced CMOS technologies such as 65 nm and 45 nm processes can further reduce chip area and increase operating speed, although they introduce challenges such as increased leakage currents.Artificial intelligence-based design optimization techniques, including machine learning algorithms and evolutionary optimization methods, may be used to automate transistor sizing and improve design efficiency. Adaptive biasing techniques can also be implemented to dynamically adjust bias currents based on signal conditions, thereby improving energy efficiency. Another important direction involves the integration of analog sensing circuits with digital processing units on a single chip using System-on-Chip (SoC) architectures. This approach enables highly compact and intelligent sensing systems for edge computing applications.Future operational amplifier designs will also play a critical role in emerging fields such as edge artificial intelligence, secure hardware systems, and implantable biomedical electronics. The ongoing evolution of ultra-low-power circuit techniques will enable the development of intelligent sensor nodes capable of operating for long periods using energy harvesting technologies.

References

[1] S. N. S. Baharudin, A. B. Jambek, and R. Che Ismail, “Design and analysis of a two-stage OTA for sensor interface circuits,” in *Proceedings of the IEEE Symposium on Computer Applications & Industrial Electronics (ISCAIE)*, Penang, Malaysia, Apr. 2014, pp. 1–6.

[2] G. Palmisano, G. Palumbo, and S. Pennisi, “Design procedure for two-stage CMOS transconductance operational amplifiers: A tutorial,” *Analog Integrated Circuits and Signal Processing*, vol. 27, pp. 179–189, 2001.

[3] S. Malipatil, “Review and analysis of glitch reduction techniques for low-power VLSI circuits,” *International Journal for Research in Applied Science & Engineering Technology (IJRASET)*, vol. 5, no. 2017, ISSN: 2321-9653.

[4] N. Naveena, N. Poojitha, P. Rageshwari, and S. Malipatil, “Low power digital circuits design using 120 nm technology,” *International Journal of Scientific & Technology Research (IJSTR)*, vol. 9, no. 4, pp. 1–6, Apr. 2020.

[5] S. Malipatil and A. Patil, “Design of a low-power flip-flop using MTCMOS technique in Cadence tool,” *International Journal of Ethics in Engineering & Management Education*, vol. 1, no. 4, pp. 1–5, Apr. 2014.

[6] N. Naveena, N. Poojitha, P. Rageshwari, and S. Malipatil, “Low-power and area-efficient digital circuit design for portable devices using GDI technique,” *Journal of Xidian University*, vol. 14, no. 6, pp. 1–8, 2020. doi:10.37896/jxu14.6/212.

[7] S. Malipatil, “Design of a low-power D flip-flop using AVL technique,” *International Journal of Advanced Research in Computer and Communication Engineering*, vol. 4, no. 9, pp. 300–304, Sep. 2015. doi:10.17148/IJARCCE.2015.4962.

[8] J. Zhang, W. Zhuo, and C. Ma, “A CMOS transimpedance amplifier with broadband and high gain based on negative Miller capacitance,” *Integration, the VLSI Journal*, vol. 91, pp. 60–66, 2023. doi:10.1016/j.vlsi.2023.03.004.

[9] V. Niranjan and M. Jhamb, “Design of a low-power 180 nm broadband CMOS

transimpedance amplifier for biomedical and IoT applications," *International Journal of Information Technology*, vol. 15, no. 5, pp. 2741–2745, 2023. doi:10.1007/s41870-023-01315-6.

[10] Y. Takahashi, D. Ito, M. Nakamura, A. Tsuchiya, T. Inoue, and K. Kishine, "Low-power regulated cascode CMOS transimpedance amplifier with local feedback circuit," *Electronics*, vol. 11, no. 6, p. 854, 2022. doi:10.3390/electronics11060854.

[11] J. H. Yeom, K. Park, J. Choi, M. Song, and S. Y. Kim, "Low-cost and high-integration optical time domain reflectometer using CMOS technology," in *Proceedings of the Conference on Ph.D Research in Microelectronics and Electronics (PRIME)*, Lausanne, Switzerland, 2019, pp. 145–148. doi:10.1109/PRIME.2019.8787851.