DIRECT VOLTAGE CONTROLLED DG WITH SPWM TECHNIQUE FOR MICRO-GRID APPLICATIONS

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ABSTRACT

This paper exhibits two add-on features for the voltage control scheme of directly voltage-controlled distributed energy resource units (VC-DERs) of microgrid to provide overcurrent and overload protection with sinusoidal pulse width modulation (SPWM) technique. The overcurrent protection scheme detects the fault, limits the output current magnitude of the DER unit, and restores the microgrid to its normal operating conditions subsequent to fault clearance. The overload protection scheme limits the output power of the VC-DER unit. A reenactment and equipment investigation of the proposed topology has been finished by utilizing MATLAB/SIMULINK.

Keywords: Autonomous microgrids, inverter, SPWM control.

1. INTRODUCTION

The inverters are likewise assuming a vital part in different renewable vitality applications as these are utilized for framework association of Wind Energy System or Photovoltaic System. Notwithstanding this, the control methodologies utilized as a part of the inverters are additionally like those in DC-DC converters. Both current-mode control and voltage-mode control are utilized in useful applications.

The DC-AC inverters ordinarily work on Pulse Width Modulation (PWM) system. The PWM is an extremely progress and valuable system in which width of the Gate heartbeats are controlled by different components. PWM inverter is utilized to keep the yield voltage of the inverter at the evaluated voltage (contingent upon the client's decision) regardless of the yield load. In a traditional inverter the yield voltage changes as indicated by the adjustments in the heap. To invalidate this impact of the evolving loads, the PWM inverter right the yield voltage by changing the width of the beats and the yield AC relies on upon the exchanging recurrence and heartbeat width which is balanced by estimation of the heap associated at the yield to give steady evaluated yield. The inverters normally work in a heartbeat width balanced (PWM) way and switch between diverse circuit topologies, which implies that the inverter is a nonlinear, particularly piecewise smooth framework. Notwithstanding this, the control systems utilized as a part of the inverters are additionally like those in DC-DC converters.

Both current-mode control and voltage-mode control are utilized in commonsense applications. In the most recent decade, investigations of complex conduct in exchanging force converters have picked up progressively more consideration from both the scholastic group and industry. Different sorts of nonlinear phenomena, 3, for example, bifurcation, disorder, fringe crash and existing together attractors, have been uncovered. Past work has primarily centered around DC power supply frameworks including DC-DC converters and AC-DC force component adjustment (PFC) converters.

Fig. 1: Block Diagram

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This paper is sorted out as takes after. Segment 2 depicts a general voltage control plan for a VC-DER unit. Segments 3 and 4 portray the proposed overcurrent and over-burden security plans, individually. Area 5 displays the reenactment results. Area 6 finishes up the paper.

2. A GENERAL VOLTAGE CONTROL SCHEME FOR A VC-DER UNIT

Here Fig. 2 represents a VC-DER unit, spoke to by a dc voltage source, a VSC, and an arrangement RL channel. The unit is interfaced to the microgrid at the purpose of association (PC in Fig. 1) through a stage up transformer. The square indicated by "Rest of Microgrid" in Fig. 1 incorporates current- and/or force controlled DER units and different segments, e.g., dissemination lines, burdens, and capacitor banks.

![Fig. 2: Schematic outline of a DER unit that controls the voltage at PC](image)

A square chart of a general direct voltage control plan is represented in Fig. 3. The control target is to keep up the PC voltage at its set point, with zero enduring state lapse. The control capacity is performed in the dq casing of reference. Three-stage immediate voltages of the PC transport, vabc, are measured and changed to a dq edge of reference, Vdq, and gave to the control square. The controller yields, Vt,dq, are changed to abc casing of reference considering the turns proportion and stage movement of the interface transformer. At that point, the PWM signs are created taking into account the controller yields, vt,abc, to combine the voltage at the terminal of the interface VSC. Since the control plan incorporates no internal current control circle, the VC-DER unit is liable to over current and over-burden amid framework strange conditions, e.g., flaws. Points of interest and normal uses of the control technique for a multi-DER microgrid have been accounted for and compressed in Section 5-A.

3. OVERCURRENT PROTECTION SCHEME

The targets of the over current assurance plan are to

1) Limit the yield current of the VC-DER units amid issue conditions by adjusting voltage controller yields and
2) Restore the controller after shortcoming freedom. The over current insurance plan is initially portrayed for a microgrid with a solitary VC-DER unit and after that summed up for a microgrid with numerous VC-DER units. Both arrangement L and LCL air conditioning side channel setups are considered.
Microgrid with a single VC-DER unit

The proposed over current insurance plan comprises of the accompanying. Fault Detection: An over current condition is recognized in light of the element phasor examination [27] by computing the extent of the VC-DER yield current element phasor

$$|I| = \left| \frac{V_t - V}{R + jX} \right| = \frac{|\Delta V|}{|R + jX|}$$  \hspace{0.5cm} (1)

Fig. 4: Dynamic phasor of a VC-DER unit, relating VSC terminal and PC voltages

where \( V = V_d + jV_q \) and \( V_t = V_{td} + jV_{tq} \) are the element phasors at the PC and the voltage controller yield, Fig. 1.

The PC voltage drops amid an issue condition, and the voltage controller, because of the drop, builds \( V_t \) in Fig. 3, which thus builds \( I \). The deficiency is distinguished when the yield current greatness of the DER unit, computed taking into account (1), compasses to its most extreme breaking point of \( I_{max} \).

Fault Current Limiting Scheme

To keep an extreme yield current, the yields of the controller, \( V_t, dq \) in Fig. 2, are overridden when a flaw is identified, and the VSC terminal voltage is situated to \( V_{t,mod} \), Fig. 3. The circle in Fig. 3 incorporates all VSC terminal voltage values that outcome in satisfactory yield current sizes. \( V_{t,mod} \) is ascertained in view of 1) the deliberate PC dynamic voltage phasors, \( V \), 2) the impedance between the converter terminal and the PC transport, \( R + jX \), and 3) the observed prefault yield current of the DER unit, \( I_{pf} \).

$$V_{t,mod} = V + (R + jX) \frac{I_{pf}}{\epsilon_{tran}}.$$ \hspace{0.5cm} (2)

Hence, \( I_{pf} \) is to keep the framework working point as close as could be expected under the circumstances to the prefault conditions and minimize microgrid drifters after the deficiency leeway. Steady ctran > 1 is to adjust for the rotting dc part of the immediate current that is not considered by the element phasor investigation. In light of an expansive number of contextual analyses, ctran = 3 is chosen which brings about acceptable execution even under most pessimistic scenario situations. Amid the time period that the over current security plan is dynamic, the PC voltage can altogether go astray from the reference set point in which case the voltage controller collects slip in its integrator states. This "vital windup" can bring about over the top overshoot, and subsequently an unsatisfactory transient reaction after the voltage controller is restored. To evade this circumstance, the integrator conditions of the voltage controller are solidified when the overcurrent security plan is dynamic and discharged resulting to the issue leeway.
Fault Clearance Determination and Controller Restoration

After the issue freedom, the PC voltage builds, $|I|$ drops beneath the point of confinement $I_{\text{max}}$, and the flaw leeway is recognized. At that point, the voltage controller is enacted to restore voltage following.

![Image of PC voltage greatness amid a solitary stage to ground flaw condition and its lower conceal](image)

**Fig. 5:** PC voltage greatness amid a solitary stage to ground flaw condition and its lower conceal

**Microgrid with multiple vc-der units**

This area sums up the proposed overcurrent security plan for a microgrid with different VC-DER units. The issue identification and the flaw current confinement plans portrayed in segment III- An are similarly appropriate to the VC-DER units of a microgrid that incorporates numerous DER units. Nonetheless, the flaw freedom determination and controller rebuilding phases of each VC-DER unit require further upgrade. The reason is that the present greatness of the circulation line is touchy to the voltage contrast between its two end transports, because of line little impedance. Subsequently, if the controllers neglect to keep up the voltage of the relating PC transports at the set focuses, the line current can surpass the DER yield current utmost.

In a microgrid with numerous VC-DER units, PC voltages can essentially float from their set point qualities amid a flaw, and in this manner voltage controllers need extra time to restore the PC voltages to the prefault set focuses. Interim, current extent can temporarily surpass the allowable quality. To maintain a strategic distance from accidental deficiency discovery as an aftereffect of current overshoots, resulting to a shortcoming leeway, the voltage controllers ought to be step by step restored to minimize current drifters. The accompanying depicts the flaw freedom determination and smooth controller reclamation for different VC-DER units.

**Fault clearance determination**

Deficiency freedom moment is resolved in view of the PC voltage extent $V_{\text{mag}}$ which drops amid the deficiency and begins expanding instantly after the shortcoming leeway.

$$V_{\text{mag}} = \sqrt{V_d^2 + V_q^2}$$  \hspace{1cm} (3)

Deficiency freedom is recognized when $V_{\text{mag}}$ has expanded to a predefined level. It ought to be noticed that the immediate voltage greatness, figured in view of (3), is liable to oscillatory segments amid lopsided flaws. In this manner, the lower envelope of $V_{\text{mag}}$ is checked, and the flaw leeway is recognized when this envelope has expanded to a predefined quality. Fig. 5 demonstrates an average PC voltage extent and its lower envelope for a solitary stage to ground deficiency, where $V_{\text{mag}}$ displays twofold recurrence motions. To build $V_{\text{env}}$, the base of every twofold recurrence cycle is recognized, and the envelope is situated to the base for the following twofold recurrence cycle. The issue leeway is recognized when

$$\frac{V_{\text{env}} - V_{\text{env, min}}}{\sqrt{V_{d, \text{ref}}^2 + V_{q, \text{ref}}^2}} \times 100 > \gamma$$  \hspace{1cm} (4)

where $V_{\text{env, min}}$ is the worldwide least of the envelope, and $\gamma$ is the rate increment of $V_{\text{env}}$ concerning the reference voltage set point. The reference voltage set point is chosen following the genuine voltage of a defective transport can be near to zero. Selecting higher qualities for $\gamma$ guarantees solid issue freedom determination; in any case, it decreases the reclamation speed.
Voltage control restoration

Rebuilding strategy starts after the shortcoming freedom. This methodology is a fundamental piece of the overcurrent assurance plan for a microgrid with numerous VC-DER units to guarantee the controllers are easily restored and current homeless people are restricted inside of the allowable reach. The methodology relies on upon the relative contrast between the prefault and postfault working purposes of the VC-DER unit, which relies on upon the VC-DER obvious yield power, S. A1) Spr = Spost. For this situation, the prefault and postfault working focuses are pretty nearly the same. This is the situation when the flaw 1) is makeshift and clears itself with no line or era blackout, i.e., 80–90% of the flaws in dissemination frameworks [29], 2) is changeless however its freedom does not altogether change the DER unit yield power. A2) Spr = Spost. For this situation, the postfault working point fundamentally strays from the prefault working point. This is the situation when the issue freedom involves a critical change in the DER unit yield power. To figure out which one of the above has happened, the yield current of the VC-DER, which was constrained to Ipf in [29], is continuously expanded to Irs at which the greatness of the relating PC voltage is practically the same as the prefault size. The relative contrast in the middle of Irs and Ipf is ΔI is contrasted and a resilience level, Δtol, to figure out which one of the above conditions holds. Δtol relies on upon the framework and the controllers parameters. Taking into account broad contextual analyses, Δtol = 0.1 is chosen for the reported studies.

To oblige reclosure operations, the overcurrent insurance plan holds up in reclamation state until the microgrid assurance plan recognizes the reclosure operation has been finished. Contingent upon which one of A1 or A2 conditions holds, the overcurrent assurance plan continues to restore the ordinary voltage control as takes after. A1 holds) For this situation, Vf has been as of now changed such that yield current of the VC-DER unit is Ip, and the framework ought to be sufficiently given time to achieve its consistent state. Since the postfault working point is practically indistinguishable to the prefault working point and the state variables of the controllers were solidified amid the issue and the reclamation arranges, the controller is easily restored.

A2 holds) For this situation, the controller rebuilding may bring about temperate overshoot of the VC-DER yield current which thus can be erroneously translated as an issue condition. To maintain a strategic distance from this situation and accomplish a controller smooth reclamation without current drifters, the VC-DER whose word has significantly has essentially changed is briefly disengaged, and after that the accompanying two stages are taken:

1) The voltage reference for the controller is situated at the current PC voltage.
2) The state variables of the controller are introduced such that the yields of the controller previously, then after the fact its rebuilding are meet. This is accomplished by a state eyewitness which is planned in light of the state-space parameters of the voltage controller A, B, C, and D in Fig. 3. The spectator inputs are 1) Vtd and Vtq toward the end of rebuilding stage, 2) the deliberate PC voltage, and 3) the reference set focuses. The yield of the eyewitness is the state vector x that decides the introductory conditions for the state variables of the voltage controller. The voltage controller then gets redesigned set focuses from the force administration framework (PMS) and gives following. The VC-DER unit can be therefore reconnected to the microgrid in light of an order from the PMS. Fig. 5 shows a flowchart of the voltage control plan, including the overcurrent security instrument.

Vc-der units with lcl filters

The interface VSC channel is either an arrangement RL channel, Fig. 1, or a T-shape LCL channel, Fig. 6. The proposed overcurrent security plan of Section 3-A likewise can be promptly connected to a DER unit with a T-shape LCL channel by supplanting (1) and (2) with individually, where (6) and (7) are determined in light of element phasor examination of the circuit of Fig. 6.

\[
|I_{in}| = \frac{V_f \left( \frac{X_{L1} + X_{L2}}{X_L} \right) - V}{X_{L1} + X_{L2} + \frac{X_{L1}X_{L2}}{X_C}}
\]

\[
V_{f,mod} = \frac{I_{f,req} \left( \frac{X_{L1} + X_{L2} + \frac{X_{L1}X_{L2}}{X_C}}{1 + \frac{X_{L2}X_C}{X_L}} \right) + V}{1 + \frac{X_{L2}X_C}{X_L}}
\]
4. OVERLOAD PROTECTION

The target of the over-burden security plan is to breaking point the yield force of a VC-DER unit whose controller does exclude an inward current control circle. The momentary three stage evident yield force of the DER unit of Fig. 1, in light of element phasors, is communicated as

\[
S = 3V I^* - 3V \left[ \frac{V}{R + jX} \right] = 3V \left[ \frac{\Delta V}{R + jX} \right]. \tag{8}
\]

Taking into account the most extreme era limit of the unit, Smax, the impedance R + jX, and the PC voltage V, the greatest greatness of the voltage contrast, ΔVmax, that compares to the most extreme yield force is

\[
\Delta V_{\text{max}} = \frac{S_{\text{max}}}{3|V|}. \tag{9}
\]

Thus, the VC-DER unit is overloaded if |ΔV| > ΔVmax and leads to the following overload protection strategy. The magnitude

\[
|\Delta V| = \sqrt{(V_{id} - V_d)^2 + (V_{iq} - V_q)^2} \tag{10}
\]

is contrasted and ΔVmax. On the off chance that |ΔV| > ΔVmax, the yield of the voltage controller is over looked, and the terminal voltage, in the dq reference edge, is allocated in light of (9) and the deliberate PC voltage Vdq. The region inside of the circle of Fig. 3 recognizes all |ΔV| that outcome in satisfactory yield power. To boost the yield force of the unit, ΔV with the size of ΔVmax is chosen. To work as close as would be prudent to the working point that the voltage controller has determined, the edge of ΔV is chosen such that the separation between Vtיךmod and Vt difíc Fig. 3, is minimized, i.e.,

\[
V_{id,\text{mod}} = V_d + \Delta V_{\text{max}} \cos \left( \tan^{-1} \frac{V_{iq} - V_q}{V_{id} - V_d} \right)
\]

\[
V_{iq,\text{mod}} = V_q + \Delta V_{\text{max}} \sin \left( \tan^{-1} \frac{V_{iq} - V_q}{V_{id} - V_d} \right). \tag{11}
\]

This will confine the yield force of the DER unit to Smax. When the yield force is restricted, the integrator conditions of the voltage controller are kept unaltered to keep away from fundamental windup. The microgrid PMS determines the over-burdening state of the DER unit as quick as would be prudent, e.g., by either load shedding or force stream adjustment. The voltage controller can then be restored, and since the basic windup has been kept away.

5. CONTROL TECHNIQUE

The advent of the transformer less multilevel inverter topology has brought forth various pulse width modulation (PWM) schemes as a means to control the switching of the active devices in each of the multiple voltage levels in the inverter. The most efficient method of controlling the output voltage is to incorporate pulse width modulation control (PWM control) within the inverters. In this method, a fixed d.c. input voltage is
supplied to the inverter and a controlled a.c. output voltage is obtained by adjusting the on and–off periods of the inverter devices. Voltage-type PWM inverters have been applied widely to such fields as power supplies and motor drivers. This is because: (1) such inverters are well adapted to high-speed self turn-off switching devices that, as solid-state power converters, are provided with recently developed advanced circuits; and (2) they are operated stably and can be controlled well.

The PWM control has the following advantages:

- The output voltage control can be obtained without any additional components.
- With this type of control, lower order harmonics can be eliminated or minimized along with its output voltage control. The filtering requirements are minimized as higher order harmonics can be filtered easily.
- The commonly used PWM control techniques are:
  - Sinusoidal pulse width modulation (sin PWM)
  - Space vector PWM

The performance of each of these control methods is usually judged based on the following parameters: a) Total harmonic distortion (THD) of the voltage and current at the output of the inverter, b) Switching losses within the inverter, c) Peak-to-peak ripple in the load current, and d) Maximum inverter output voltage for a given DC rail voltage. From the above all mentioned PWM control methods, the Sinusoidal pulse width modulation (sinPWM) is applied in the proposed inverter since it has various advantages over other techniques. Sinusoidal PWM inverters provide an easy way to control amplitude, frequency and harmonics contents of the output voltage.

**Sinusoidal Pulse Width Modulation**

In the Sinusoidal pulse width modulation scheme, as the switch is turned on and off several times during each half-cycle, the width of the pulses is varied to change the output voltage. Lower order harmonics can be eliminated or reduced by selecting the type of modulation for the pulse widths and the number of pulses per half-cycle. Higher order harmonics may increase, but these are of concern because they can be eliminated easily by filters. The SPWM aims at generating a sinusoidal inverter output voltage without low-order harmonics. This is possible if the sampling frequency is high compared to the fundamental output frequency of the inverter.

Sinusoidal pulse width modulation is one of the primitive techniques, which are used to suppress harmonics presented in the quasi-square wave. In the modulation techniques, there are two important defined parameters: 1) the ratio $P = f_c/f_m$ known as frequency ratio, and 2) the ratio $M_a = A_m/A_c$ known as modulation index, where $f_c$ is the reference frequency, $f_m$ is the carrier frequency, $A_m$ is reference signal amplitude and $A_c$ is carrier signal amplitude.

By varying the modulation index $M$, the RMS output voltage can be varied. It can be observed that the area of each pulse corresponds approximately to the area under the sine-wave between the adjacent midpoints of off periods on the gating signals.

**6. SIMULATION RESULTS**

**Simulation Parameters**

- Distributed source, DC Supply=100V
- Grid model: 11KV, 50Hz 100MVA
- Metal-oxide semiconductor FET:
  - $R_{ON}=0.1$ Ohm
  - $V_{fd}=0V$
- Snubber:
  - $R_s=0.1$MOhm
  - $C_s=\text{inf}$

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a) DG input voltage

Sinusoidal PWM parameters
Carrier Frequency= 1080Hz
Modulation index, m=0.6
Output frequency, f0=50Hz

Transformer selection at inverter output terminals
Inverter output voltage is around =50V, 50Hz
Grid integration voltage= 415V (L-L rms), 50Hz
So,
Transformer needed= 100V/415V, 50Hz

b) Inverter Output

c) Transformer output voltages and with GRID interconnection

d) Transformer output current and with GRID interconnection

7. CONCLUSION

Distributed energy resources are utilized in micro grid applications. This is connected through 415V grid through a voltage source inverter, which employs SPWM technique. compared to convectional system amount of losses incurred in the system are reduced by employing sinusoidal PWM technique.
REFERENCES


