DESIGN OF A CURRENT MIRROR BASED DIFFERENTIAL AMPLIFIER FOR LOW-VOLTAGE AND LOW POWER APPLICATIONS

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ABSTRACT

As per the Moore’s law, there is an extreme increase in number of on chip devices, this increase in chip density results in power dissipation and thus the power utilization is unsatisfactory. So to avoid this problem the concept of Low Power system arises. As a part of microelectronics, it has been proposed to make the choice of minute circuit with attraction added by use of MOS cells. Since we often use operational amplifiers in our specialty, we chose to recreate an operational amplifier from templates provided in the book Basics of CMOS Cell design. Nowadays, differential amplifiers are widely employed in many circuits. If we minimized the power consumption of a single differential amplifier the power consumption of the whole circuit will be considerably minimized. In this paper, analysis of the Inverter based differential amplifier and the current mirror circuit based amplifier design are shown. Thus, the purpose of this paper is to design an advanced differential amplifier circuit using CMOS technology with lesser power consumption & high Gain.

Keywords: CMOS, Differential Amplifier, power dissipation.

INTRODUCTION

Comparators are the second most widely used electronic components after operational amplifiers in recent technologies. They are known as 1-bit analog-to digital converters and thus they are mostly used in large abundance in A/D converters. In the analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. The conversion speed of comparator is limited by the decision making response time of the comparator. As the comparator is one which limits the speed of the converter, its optimization is of utmost importance. In today’s world, where demand for portable battery operated devices is increasing, a major thrust is given towards low power methodologies for high-speed applications. This reduction in power can be achieved by moving towards smaller feature size processes. However, as we move towards smaller feature size processes, the process variations and other non-idealities will greatly affect the overall performance of the device. One such application where low power dissipation, low noise, high speed, less hysteresis, less Offset voltage are required is Analog to Digital converters for mobile and portable devices. The performance limiting blocks in such ADCs are typically inter-stage gain amplifiers and comparators. The accuracy of such comparators, which is defined by its offset, along with power consumption, speed is of keen interest in achieving overall higher performance of ADCs. In the past, pre-amplifier based comparators have been used for ADC architectures such as flash and pipeline. The main drawback of pre-amplifier based comparators is the more Offset voltage. To overcome this problem, dynamic comparators are often used that make a comparison once every clock period and require much less offset voltage. However, these dynamic comparators suffer from large power dissipation compared to pre-amplifier based comparators. The main problem with all these dynamic comparators is the output signal of the latch stage is fluctuating during clock transition. This is happening due to the presence of noise in input terminals.

PURPOSE OF STUDY

Traditional operational amplifier designs most commonly use transistors in the saturation region, which generally requires at least one DC bias current. As technology size has decreased, low power, high gain
amplifier design has become more challenging for designers. Since transistor threshold voltage generally doesn’t decrease as fast as feature size and power supply voltage, many cascaded or folded designs are not possible with reduced voltage supply. Given that the reduction in headroom reduces the ability to cascade devices, low voltage high-gain amplifiers are commonly built by expanding outward, using two or even three cascaded amplification stages. These multi-stage cascaded designs require the designer to take extra measures to ensure amplifier stability, and, depending on the topology, can be very challenging or complex to stabilize. Most stabilization schemes require additional compensation capacitors and/or nulling resistors, which use additional silicon area, and can decrease circuit bandwidth; however, these compensation reduced power supply voltage and the increasing demand for low power consumption make sub-threshold operation and design a more viable alternative when a reduction in bandwidth is acceptable. Operation in the sub-threshold region causes the drain current to increase exponentially with VGS as opposed to quadratically in the saturation region. The disadvantage with sub-threshold operation is the reduction in amplifier driving current, and the loss of ability to quickly drive large capacitive loads. In this paper, an inverter-based operational amplifier topology and operation and design principles are discussed and evaluated. We use two previously used figures of merit to objectively compare various aspects of the different circuit topologies. We conclude that the inverter-based differential amplifier topology with current starving provides one of best circuit topologies for energy efficiency. One such application where low power dissipation, low noise, high speed, less hysteresis, less Offset voltage are required is Analog to Digital converters for mobile and portable devices. The performance limiting blocks in such ADCs are typically inter-stage gain amplifiers and comparators. The accuracy of such comparators, which is defined by its offset, along with power consumption, speed is of keen interest in achieving overall higher performance of ADCs. In the past, pre-amplifier based comparators have been used for ADC architectures such as flash and pipeline. The main drawback of pre-amplifier based comparators is the more offset voltage. To overcome this problem, dynamic comparators are often used that make a comparison once every clock period and require much less offset voltage. However, these dynamic comparators suffer from large power dissipation compared to pre-amplifier based comparators. The main problem with all these dynamic comparators is the output signal of the latch stage is fluctuating during clock transition. This is happening due to the presence of noise in input terminals. In this paper we have designed all type of comparators.

Sub-threshold current is the current between the source and drain of a MOSFET when the transistor is in sub-threshold region, or weak-inversion region, that is, for gate-to-source voltages below the threshold voltage. The terminology for various degrees of inversion is described in Tsividis [1,2].

In digital circuits, sub threshold conduction is generally viewed as a parasitic leakage in a state that would ideally have no current. In micro power analog circuits, on the other hand, weak inversion is an efficient operating region, and sub threshold is a useful transistor mode around which circuit functions are designed.

In the past, the sub threshold conduction of transistors has usually been very small in the off state, as gate voltage could be significantly below threshold; but as voltages have been scaled down with transistor size, sub-threshold conduction has become a bigger factor. Indeed, leakage from all sources has increased: for a technology generation with threshold voltage of 0.2 V, leakage can exceed 50% of total power consumption [3].

The reason for a growing importance of sub threshold conduction is that the supply voltage has continually scaled down, both to reduce the dynamic power consumption of integrated circuits (the power that is consumed when the transistor is switching from an on-state to an off-state, which depends on the square of the supply voltage), and to keep electric fields inside small devices low, to maintain device reliability. The amount of sub threshold conduction is set by the threshold voltage, which sits between ground and the supply voltage, and so has to be reduced along with the supply voltage. That reduction means less gate voltage swing below threshold to turn the device off, and as sub threshold conduction varies exponentially with gate voltage (see MOSFET: Cut-off Mode), it becomes more and more significant as MOSFETs shrink in size [4]. Sub threshold conduction is only one component of leakage; other leakage components that can be roughly equal in size depending on the device design are gate-oxide leakage and junction leakage [5]. Understanding sources of leakage and solutions to tackle the impact of leakage will be a requirement for most circuit and system designers. To reduce the sub threshold effect here we use the stacking scheme and design of inverter based amplifier was proposed.
Fig 1: Inverter Based amplifier Design

The inverter-based amplifier topology shown in Figure 1 uses CMOS inverters as the amplifier input. This input stage design has the advantage of combining the transconductance of the n and p transistors.

This combination of the two transconductances should provide 6dB increase in gain over a traditional common source amplification stage, with approximately the same DC bias current. When this architecture is implemented with a standard supply voltage (>2vt), the overall transconductance can be increased significantly depending on how transistors in the inverters are sized and the resulting current through the inverter. High current through the inverter allows significantly high bandwidths to be achieved. Another advantage of this topology is an increase in output swing and linearity when compared to a traditional common source or cascade amplifier if the respective transconductances of the p and n type transistors are approximately equal in magnitude. For noise, the inverter-based topology offers lower equivalent noise resistance compared to the equivalent common source topology.

Sub-Threshold Operation with Current Starving Tails

When this inverter-based architecture is implemented at a low supply voltage (<2vt), the inverter transistors will operate in the sub-threshold region. Because of this region of operation, bias currents and power consumption can be significantly reduced, with the sacrifice of bandwidth and amplifier driving strength. A tail current source can be added to better control the current flow through the inverters, pushing the transistors further into the sub-threshold region, and further reducing power consumption. The tail can also improve the amplifier’s CMRR and provide an additional input that can be used for common-mode feedback, circumventing the issue with the original inverter-based previous designs. In addition, the use of tail separates the need for low power consumption and low input offset voltage. Inverters can be sized appropriately to control offset voltage while the tail controls the overall power consumption allowed by the inverter.

Fig 2: Inverter Op-Amp With Tails
The proposed topology shown in Figure 2 employs an active load consisting of four additional load inverters (M2, M3). The innermost pair of these inverters is connected in a cross-coupled configuration, while the outer pair of inverters is diode-connected as shown in Figure 3. The cross coupled pair provides positive feedback and therefore a negative resistance of \(-2/gm3\). The diode connected pair provides an equal, yet positive resistance of \(2/gm2\).

**PROPOSED DESIGN**

The new approach of analog circuit techniques that is compatible with future CMOS technologies. There are several important advantages of this approach. First, the need to develop expensive CMOS technologies with lower threshold voltages is avoided. Secondly, high efficiency dc-dc converters are not required. Thirdly, circuit techniques that permit low voltage operation with large thresholds offer the potential for more fully utilizing the technology at higher voltages and at lower voltages if, in fact, low threshold technologies do become standard technologies.

**Need of Low voltage circuits**

1. As the device channel length is scaled down into submicrons and the gate oxide thickness becomes only several nanometer thick, the supply voltage has to be reduced in order to ensure device reliability. With deep submicron processes now available, the maximum allowable supply voltage is decreasing from 5V to 3V and even to 2V.
2. The increasing density of the components on chip dictates low power. A silicon chip can only dissipate a limited amount of power per unit area. Since the increasing density of components allows more electronic functions per unit area, the power per electronic function has to be lowered in order to prevent overheating.
3. Portable, battery-powered equipment needs low power to ensure an acceptable operation period from a battery, and the supply voltage must be as low as possible to reduce the number of batteries used.

The main purpose of the input stage in Op Amp is to amplify differential signals and reject common-mode input voltages. An important specification of an input stage is the common mode input range. If the common mode voltage is kept within this range, the input stage will properly respond to small differential signals. Hence an application has to be designed such that the common mode input voltage stays within the common-mode input range.

**Proposed comparator design**

Design has current mirror based comparator which significantly helps in maintaining current in the circuit constant regardless of loading. The active load consists of cross-coupled inverter pair which has a great impact.
in improving the gain of the circuit. Irrespective of the load given, the current mirror circuit drives the output to an optimum level. $V_{CMFB}$ connected to current tail acts as a controller circuit to the voltage gain of the whole circuit.

**SIMULATION**

The Inverter Based op-amp and the proposed op-amp are designed and simulated using TSMC018 technology in Tanner Tools.

**Table 1: Power dissipation values**

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Power Dissipation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverter based Op-Amp</td>
<td>2.358181e-003 watts</td>
</tr>
<tr>
<td>Proposed Op-Amp</td>
<td>1.274639e-003 watts</td>
</tr>
</tbody>
</table>

**CONCLUSION**

A method is presented to efficiently compensate buffered Op- Amps. In this approach, the OTA is compensated by connecting a capacitance between the input and output of the buffer. This configuration results in a significant improvement both in the unity gain frequency and phase margin, providing higher speed and improved stability. A fully-differential Op-Amp is designed in a TSMC018 standard digital CMOS process using the proposed compensation scheme. The total power consumption of the Op-Amp is reduced when compared to the existing techniques.

**REFERENCES**